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EUROPEAN PARTNERSHIP

APPENDIX 4: ACTIVITIES LAUNCHED IN 2024 FOR THE INITIATIVE PART

Version 12

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1. ACTIVITIES 2024 INITIATIVE PART

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2. DIGITAL-Chips-2024-CSA-CCC-2: Support to the European Network of Chips Competence Centres
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2. NATIONAL BUDGETS FOR THE INITIATIVE CALLS 2024

Participating states	Chips-2024-CCC	Chips-2024-CPL-5	Chips-2024-CDP-1	Chips-2024-QAC-1	Chips-2024-QAC-2	Total (M€)
AT						
BE-FL						
BE-BR						
BE-WL						
BG						
CY						
CZ						
DE						
DE TH						
DE SN						
DK						
EE						
EL						
ES AEI						
ES MAETD						
FI						
FR						
HR						
HU						
IE						
IL						
IS						
IT MIMIT						
IT MUR						
LT	2	0	0	0	0	2
LV	0,74	0	0	0	0	0,74
LU						
MT						
NL	8	66,3	0	10	0	84,3
NO	4	0	0	0	0	4
PL						
PT						
RO						
SE						
SI	2					
SK						
TR						

UK						

All budgets are indicated in Million Euros (€)

3. TECHNICAL DESCRIPTION OF THE CALLS

3.1. Chips-2024 CCC-1: Competence centres

Chips-2024-CCC-1	
DIGITAL-Chips-2024-SG-CCC-1	EU Expenditure = ***Max. EURO 116 Mio***
Security	***Call restricted on the basis of Article 12(6) of the Regulation (EU) 2021/694[1]***
Publication date	***04th Jul 2024***
Deadline Submission of proposals	***2nd Oct. 2024 at 17:00 Brussels Time***

3.1.1. Context

Competence centres in semiconductors (aka "Chips Competence Centres" or "Chips CCs") will play an essential role in the Chips for Europe Initiative. The centres will provide access to technical expertise and experimentation in the area of semiconductors, helping companies, SMEs in particular, to approach and improve design capabilities and developing skills. Competence centres will provide services to semiconductor stakeholders, especially targeting start-ups and SMEs. Examples include facilitating access to pilot lines and to the European virtual design platform, providing training and skills development, support to finding investors, making use of existing local competencies or reaching out to relevant vertical sectors. The services should be provided on an open, transparent and non-discriminatory basis. Each competence centre should connect and be part of the European network of competence centres in semiconductors and should act as an access point to other nodes of the network.

3.1.2. Expected outcomes

The competence centres shall

- **promote the actions** developed by the Chips JU in the frame of the Chips for Europe Initiative as well as the success stories.
- be a **first entry point for** users (mainly SMEs and startups) and guide users in accessing the other infrastructures set up by the Chips JU under the Initiative: the design platform and the pilot lines.
- be essential in **facilitating skill development activities.**
- support companies in **accessing the Chips Fund**.

1 Refer to Annex IV for further information on the application of this article.

- Perform other activities that can help European organizations (mainly SMEs and startups) to develop their activities in the frame of the Chips for Europe initiative and vice versa support the consortia that implement the pilot lines and the design platform to reach out to the larger community of organizations that could profit from those efforts.

3.1.3. Scope

Chips CCs should have a **specialised area of expertise**. Each competence centre decides on its specialisation in a certain technology, domain, or set of activities. It should be reflecting the specialisation of the stakeholders of that area / Participating State and should push innovation in that area within the Union. Examples of areas of expertise are Chips for medical devices, power electronics, cutting-edge semiconductors, heterogeneous integration, packaging, metrology, EDA simulation tools, Chips for automotive, silicon photonics and photonic integrated circuits, quantum Chips, system design, etc.

Chips CCs shall offer several **support activities**. Offering such support activities is common to all Chips CCs and is a necessary characteristic to belong to the network of competence centres. Support activities can be:

- **Awareness raising, promoting services, promoting success stories**: the services offered by Chips CCs may be new and may not be well recognised in the beginning. Therefore, Chips CCs need to raise awareness about their services, need to promote their services, and may need to develop an outreach program to promote the Chips CC services to potential user companies, esp. smaller enterprises. Chips CCs may need to go to many events in their countries to increase familiarity of their services with their target customers. They may need to target specific vertical sectors. They may need to promote success stories that show how their services benefit their customers. They may need to hire staff with the right soft skills to interact with customers and provide the interface between technical Chips CC staff and customers.
- **Facilitate access to the design platform and to pilot lines** by providing information and support on how to access the platform or the pilot lines when users do not have the knowledge or expertise to do so directly.
- **Support interested users in developing semiconductor solutions (technology transfer)** by supporting technology transfer activities at local/regional/national level and – where needed – at EU level. Research activities as well as operation, administration or procurement of infrastructures are not within the scope of Chips CCs, but competence centres are expected to advise on such activities and support knowledge

transfer e.g. from relevant R&I initiatives to the local semiconductor ecosystem. Support could also be in the form of matchmaking between a research organization and a user.

- In addition, Chips CCs could grant facilitated access to experts in such areas as legal compliance and business development. They may offer assistance to SMEs in creating business plans and conducting market studies.
- **Providing (access to) training on skills**: Advanced training on specific design and manufacturing skills and practices is often difficult to access for SMEs and other stakeholders. They need access to education services for development of skills in different disciplines but also for different audiences or levels (e.g. bachelor, masters level), access to top-level teachers, or support for the set-up of a credentials/micro-credentials framework. Chips CCs should support local and national training and skills development in the area of semiconductor technologies through face-to-face as well as online training (e.g. via MOOC platforms). Chips CCs should determine what is needed in their countries, should know the competences of other Chips CCs, and – where needed – provide trainings to other CCs ('train-the-trainer'). Trainings can be provided by CCs themselves, or by third parties hired by the centres. A variety of training models can be used, ranging from alternation model or cluster model, via on-the-job trainings and apprenticeships, to crash courses and mentoring programmes.
- **Participate in the organization of a European Network of Chips Competence Centres** (**ENCCC**) **and facilitate the access to this network.** Part of the resources of a Chips CC should be dedicated to building and extending this network, in collaboration with a Coordination and Support Action (see Chips-CCC-2 : Support to the European Network of Chips Competence Centres). Chips CCs should help stakeholders, especially smaller companies such as SMEs and start-ups, to connect to other competence centres within the overall network of competence centres. They should provide stakeholders with information on relevant competences in the network as well as on national and international programs, companies, and research centres in semiconductors. A Chips CC should help a stakeholder to connect to the right competence centres within the overall network of competence centres, if the local/national Chips CC does not have the right competences to support the stakeholder. In return, a Chips CC will support stakeholders from other regions and countries that need its (specialised) expertise through the network of competence centres.
- Chips CC should act as **entry points to other European initiatives**, such as the network of European Digital Innovation Hubs, HPC competence centres, cybersecurity centres, etc. The goal is to ensure that national stakeholders have access to the best

available expertise and support in Europe, by matching stakeholders' needs with the available expertise in the network of competence centres. Such expertise may be the specialisation of another competence centre and be accessible through the ENCCC.

- **Promoting the Chips Fund and facilitating access to venture capital:** SMEs and startups are often faced with insufficient financial support and have difficulties to get loans, equity, and/or grants. In particular, startups experience difficulties in managing resources and investment at the initial stage. Competence centres in semiconductors may support SMEs, startups, and other companies to access the Chips Fund. They may also support companies in finding investors, including venture capital.
- **Awareness raising, promoting services, promoting success stories**: the services offered by Chips CCs may be new and may not be well recognised in the beginning. Therefore, Chips CCs need to raise awareness about their services, need to promote their services, and may need to develop an outreach program to promote the Chips CC services to potential user companies, esp. smaller enterprises. Chips CCs may need to go to many events in their countries to increase familiarity of their services with their target customers. They may need to target specific vertical sectors. They may need to promote success stories that show how their services benefit their customers. They may need to hire staff with the right soft skills to interact with customers and provide the interface between technical Chips CC staff and customers.

Chips CCs should primarily offer services that address the needs from their prime user communities. Nevertheless, Chips CCs should also answer the needs from other organisations, e.g. from other countries, and work in close coordination and collaboration with the rest of the Network to achieve the highest possible impact, ensure the most efficient use of the CCs' resources, and to avoid duplication of efforts among the Chips CCs and with other initiatives, such as the European Digital Innovation Hubs.

3.1.4. Access to the Chips CC

Access to a Chips CC's services shall be open to several users and be granted on an **open, transparent and non-discriminatory basis**.

In line with the Chips Act, services to SMEs or public sector organisations (e.g., RTOs) could be made available **for free or against reduced prices**, and **against market prices for large companies**. Given that large enterprises need to pay the market price, they will not be considered as beneficiaries of State aid. Conversely, public entities involved in non-economic activities or exercising public authorities' functions can benefit from access granted at reduced

fees or for free, as such activities are not subject to State aid control. However, public entities (and also research organisations) when involved in economic activities, follow the same rules as applicable to large undertakings vs SMEs, i.e. they need to pay the full market price (large undertakings) or get access at reduced fees or for free (SMEs).

As a consequence, every competence centre must, in their proposal, draw up an **indicative price list for all their services, based on market prices**. The **reduction of prices** for SMEs or other eligible entities has to be made public as well, similarly to the prices charged on market terms by the competence centres. Proposals must include the methods to calculate the market price used in the price list and/or the cost of the services, so that external experts can evaluate its validity and appropriateness.

Moreover, services provided should be accessible in the national languages as well as in English.

The Chips CCs must be established as organisations with appropriate visibility to national, regional and local communities. In general, Chips CCs should employ semiconductor specialists, primarily with full-time contracts, and with expertise in areas that are most relevant for the national communities and the specialisation of their centres. A Chips CC should have an independent organisational structure and its staff should not work under external supervision.

3.1.5. Consortia for CC

A Chips CC is a **single organisation** or a **coordinated group** of organisations (consortium) with complementary expertise, established with a **non-profit objective**, aiming to promote the use of semiconductor technologies. In the case of a consortium, one organization will be appointed as coordinator. Although there is formally no limit on the number of entities setting up a competence centre, a small number of partners per Chips CC is desirable. There is no obligation for a group of organisations to create a dedicated legal entity. A Chips CC can be built on established entities in the field or can be set up from scratch.

As a matter of example, Research and Technology Organisations (RTOs) and universities could become a national competence centre of a Participating State in semiconductors. Enterprises may also set up a competence centre, or be part of a group establishing a competence centre. However, the centre must have a non-profit objective and services must be offered not-for-profit.

Candidates for competence centres are not limited to those legal entities that are involved in the set-up of pilot lines, the design platform, or are somehow involved in any other way in the Chips for Europe Initiative. Being involved in the setup and/or operation of infrastructures is not a requirement for competence centres. The Participating States have the sole and direct responsibility to propose candidate competence centres.

The Chips for Europe Initiative will support the establishment of competence centres **throughout the Union and Participating States**. The European Network of competence centres in semiconductors may comprise zero, one, or more centres per eligible country (Participating States). Participating States may decide to team up with other countries and support **cross-border competence centres**.

Typical **users** of the services offered by a Chips CC are companies, in particular local/national SMEs and startups, RTOs, and academic institutions at the regional, national and EU level. Public authorities and large enterprises may also use the services of a competence centre, but normally they are not the prime customers.

3.1.6. Size, funding and access to services

The call will be implemented as a single DEP call with open access. As a result of the evaluation of the call, selected consortia will be offered to sign a DEP grant.

The Union will make available **up to EUR 1 million per year, per country, for a 4-year period**. There is no differentiation based on country size, i.e. all countries may get the same maximum amount of EU funding per year to support their competence centres. There is also no differentiation based on the number of competence centres that a country wants to support, i.e. the maximum, annual amount of EU funding may be used to support one or more competence centres.

Participating States are expected to **co-finance** their national competence centres together with the Union, i.e. 50% will be funded through EU contributions and 50% through national contributions. Union funding is conditional on the availability of the same (or higher) amount of national contributions. Participating States may provide the same amount of maximum annual, financial contributions as the Union, i.e. EUR 1 million per year. Participating States may also opt to provide a higher amount of annual national contributions (i.e. higher than EUR 1 million per year), but this will not lead to a similar, higher annual Union contribution.

Participating States may provide a lower amount of annual national contributions (i.e. lower than EUR 1 million per year), and this will lead to a similar, lower annual Union contribution.

The EU funding for the competence centres will be made available through Digital Europe grants, which allow to fund **specific cost items**:

- Qualified personnel of the competence centre to deliver the services mentioned above to the organisations participating in a CC, including subcontracting for specialists;
- Procurement and/or depreciation costs for equipment and facilities, both hardware and software;
- Travel grants for personnel of the competence centre and local stakeholders to carry out their activities.
- Indirect costs are included as 7% of the direct cost.

3.1.7. Type of Action

DIGITAL Simple Grants – 50% **maximum** EU funding rate

3.1.8. Admissibility

Admissibility conditions are described in Annex II "General DIGITAL conditions" of this document.

Regarding page limits:

- The page limit for the chapter RELEVANCE is 20 pages
- The page limit for the chapter IMPLEMENTATION is 60 pages
- The page limit for the chapter IMPACT is 20 pages

3.1.9. Eligibility and selection process

Applications will only be considered eligible if their content corresponds wholly (or at least in part) to the topic description for which they are submitted.

Participant eligibility conditions are described in Annex II "General DIGITAL conditions" of this document.

Candidates to the consortium for a Chips CC must at least fulfil the following criteria:

- Appropriate competences to provide the services outlined above;
- Appropriate management capacity, staff and infrastructure necessary to provide the services outlined above;
- Operational and legal means to apply the administrative, contractual and financial management rules that come with a grant agreement;
- Appropriate financial viability, corresponding to the level of funds they will be called upon to manage.

The Chips JU will launch an **open call for proposals** to set up competence centres in semiconductors. To be eligible, a proposal submitted to the call will have to provide proof that the centre has been designated by its Participating State and that it will be co-financed by the Participating State. In particular, **the proposal shall include as mandatory document a letter describing the formal commitment of the Participating State,** as the one provided in Annex I to the present document.

In the **evaluation phase**, the Chips Joint Undertaking will evaluate proposals by designated candidate centres. In case a Participating State has designated more candidates than its desired number and size of competence centres, the evaluation will be competitive. Otherwise, the evaluation will be a quality assessment of designated candidates.

Eligible proposals will be evaluated according to the criteria of DEP (see Award criteria) and all those scoring above all thresholds will be ranked. Based on the ranked list, the Chips JU's Public Authorities Board will select proposals for funding. Selected proposals will get a grant from the Chips JU for a duration of 4 years.

Further details on the evaluation procedure are described in the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU[2]

3.1.10. Financial and operational capacity and exclusion

Please refer to Annex II "General DIGITAL conditions" of this document.

3.1.11. Award criteria used for open calls

The award criteria used are as follows:

2 Decision GB 2024.71

Criterion 1 - Relevance

- Alignment with the objectives and activities as described in **section 2.1 of the Chips JU Work Programme 2023-2027- Appendix 4.**
- Contribution to long-term policy objectives, relevant policies and strategies, and synergies with activities at European and national level;

Criterion 2 - Implementation

- Maturity of the proposed CC;
- Soundness of the implementation plan and efficient use of resources;
- Capacity of the applicants, and when applicable the consortium as a whole, to carry out the proposed work.

Criterion 3 - Impact

- Extent to which the project will achieve the expected outcomes and deliverables referred to in the call for proposals and, where relevant, the plans to disseminate and communicate project achievements;
- Extent to which the project will strengthen competitiveness and bring important benefits for society;

3.1.12. Score

The scores will be given with a resolution of one decimal.

Criteria	Range	Weight (**)	Threshold (*)
Relevance	0-5	1	3
Implementation	0-5	1	3
Impact	0-5	1	3
Total	0-15		10

(*) threshold applies to unweighted score.
(**) the weight is only used to establish the ranking of the proposals.

3.2. Chips-2024-CCC-2: Support to the European Network of Chips Competence Centres

Chips-2024-CCC-2	
DIGITAL-Chips-2024-CSA-CCC-2	EU Expenditure = ***Max. EURO 4 Mio***
Instrument / Type of Action	***Coordination and Support Action (DEP)***
Security	***Call restricted on the basis of Article 12(6) of the Regulation (EU) 2021/694[3]***
Publication date	***04th Jul 2024***
Deadline Submission of proposals	***2nd Oct. 2024 at 17:00 Brussels Time***

3.2.1. Expected Outcomes

The European semiconductor ecosystem will be strengthened through an effective network of Chips Competence Centres (Chips CCs) supporting the adoption and use of semiconductor technologies, in particular by SMEs, and taking into account the specific needs of the local, regional and/or national ecosystem(s). The coordinated network will facilitate access to pilot lines and the European virtual design platform and knowledge transfer within the Chips CCs. The Coordination and Support Action will ensure the European network of Chips Competence Centres will be embedded in the European semiconductor ecosystem with strong links to other European initiatives, for example, in the area of training.

Moreover, the action will result in

- Effective coordination and exchange of best practices and information among the network of Chips CCs;
- Facilitated access to services and training offered at national or regional level to interested Chips CCs and other potential users (from industry, academia or public sector);
- Maximised visibility and outreach of Chips CCs, in particular to SMEs and industry;
- Improved coordination and increased availability of training activities on semiconductor technologies across Chips CCs and within the European semiconductor ecosystem;

The main objective of the Coordination and Support Action is to maximize networking between existing European points of semiconductor knowledge and expertise. The tasks and services will provide a single focal point at European level, which will be responsible for the support of the Chips Competence Centres, the exchange of best practices among these centres, facilitating the sharing of knowledge and information, networking and training across competence centres.

3 Refer to Annex IV for further information on the application of this article.

In order to accomplish these objectives, the selected consortium should also establish effective cooperation with other European initiatives, in particular regarding skills and training in semiconductors.

3.2.2. Scope

Proposals should aim at supporting the networking among the Chips Competence Centres. In particular, it is expected to establish a communication platform, facilitate dialogue, promote the objectives of the Centres, and organize outreach events and workshops. The activities should leverage on synergies and complementarity of the centres.

The Coordination and Support Action should:

- Support the exchange of best practices among Chips CCs;
- Disseminate the activities of the Network. Maximise visibility and outreach of Chips CCs, in particular to SMEs, industry and the public sector;
- Promote the services of the Chips CCs, specifically addressing the needs of SMEs;
- Attract new users and support the engagement of industry and SMEs in the activities of the Chips CCs;
- Educate and assist Chips CCs in technology transfer practices, including IP management, where relevant;
- Define and monitor meaningful qualitative and quantitative KPIs for the European Network of Chips Competence Centres and for the Centres;
- Maintain an overview of specific specialisations and competence of the various Centres;
- Support matchmaking for specific competences;
- Facilitate access to services and training offered at national level to interested Chips CCs and other potential users;
- Support the organisation of community building events for users and Centres sharing similar interests;
- Support the connection of Chips CCs to relevant other initiatives, in particular to initiatives on skills and workforce development;
- Act as the first online point of contact for all information related to the Chips Competence Centres.

3.2.3. Type of Action

DIGITAL Coordination and Support Actions – 100% EU funding rate

3.2.4. Admissibility

Admissibility conditions are described in Annex II "General DIGITAL conditions" of this document.

Regarding page limits:

- The page limit for the chapter RELEVANCE is 20 pages
- The page limit for the chapter IMPLEMENTATION is 60 pages
- The page limit for the chapter IMPACT is 20 pages

3.2.5. Eligibility

Applications will only be considered eligible if their content corresponds wholly (or at least in part) to the topic description for which they are submitted.

Participant eligibility conditions are described in Annex II "General DIGITAL conditions" of this document.

3.2.6. Financial and operational capacity and exclusion

Please refer to Annex II "General DIGITAL conditions" of this document.

3.2.7. Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU[4].

3.2.8. Award criteria

The award criteria used are as follows:

4 Decision GB 2024.71

Criterion 1 - Relevance

- Alignment with the objectives and activities as described in **section 2.2 of the Chips JU Work Programme 2023-2027- Appendix 4.**
- Contribution to long-term policy objectives, relevant policies and strategies, and synergies with activities at European and national level;

Criterion 2 - Implementation

- Maturity of the project;
- Soundness of the implementation plan and efficient use of resources;
- Capacity of the applicants, and when applicable the consortium as a whole, to carry out the proposed work.

Criterion 3 - Impact

- Extent to which the project will achieve the expected outcomes and deliverables referred to in the call for proposals and, where relevant, the plans to disseminate and communicate project achievements;
- Extent to which the project will strengthen competitiveness and bring important benefits for society;

3.2.9. Score

The scores will be given with a resolution of one decimal.

Criteria	Range	Weight (**)	Threshold (*)
Relevance	0-5	1	3
Implementation	0-5	1	3
Impact	0-5	1	3
Total	0-15		10

(*) threshold applies to unweighted score
(**) the weight is only used to establish the ranking of the proposals

3.3. Chips-2024-CCC-3: Second call on Competence Centres

Chips-2024-CCC-3	
DIGITAL-Chips-2024-SG-CCC-3	EU Expenditure = ***Max. EURO 16 Mio***
Security	***Call restricted on the basis of Article 12(6) of the Regulation (EU) 2021/694***[5]
Publication date	***17th Dec 2024***
Call opening	***4th Feb 2025***
Deadline Submission of proposals	***4th Mar 2025 at 17:00 Brussels Time***

3.3.1. Context

Competence centres in semiconductors (aka "Chips Competence Centres" or "Chips CCs") will play an essential role in the Chips for Europe Initiative. The centres will provide access to technical expertise and experimentation in the area of semiconductors, helping companies, SMEs in particular, to approach and improve design capabilities and developing skills. Competence centres will provide services to semiconductor stakeholders, especially targeting start-ups and SMEs. Examples include facilitating access to pilot lines and to the European virtual design platform, providing training and skills development, support to finding investors, making use of existing local competencies or reaching out to relevant vertical sectors. The services should be provided on an open, transparent and non-discriminatory basis. Each competence centre should connect and be part of the European network of competence centres in semiconductors and should act as an access point to other nodes of the network.

3.3.2. Expected outcomes.

The competence centres shall

- **promote the actions** developed by the Chips JU in the frame of the Chips for Europe Initiative as well as the success stories.
- be a **first entry point for** users (mainly SMEs and startups) and guide users in accessing the other infrastructures set up by the Chips JU under the Initiative: the design platform and the pilot lines.
- be essential in **facilitating skill development activities.**
- support companies in **accessing the Chips Fund**.
- Perform other activities that can help European organizations (mainly SMEs and startups) to develop their activities in the frame of the Chips for Europe initiative

5 Refer to Annex IV for further information on the application of this article.

and vice versa support the consortia that implement the pilot lines and the design platform to reach out to the larger community of organizations that could profit from those efforts.

3.3.3. Scope

Chips CCs should have a **specialised area of expertise**. Each competence centre decides on its specialisation in a certain technology, domain, or set of activities. It should be reflecting the specialisation of the stakeholders of that area / Participating State and should push innovation in that area within the Union. Examples of areas of expertise are Chips for medical devices, power electronics, cutting-edge semiconductors, heterogeneous integration, packaging, metrology, EDA simulation tools, Chips for automotive, silicon photonics and photonic integrated circuits, quantum Chips, system design, etc.

Chips CCs shall offer several **support activities**. Offering such support activities is common to all Chips CCs and is a necessary characteristic to belong to the network of competence centres. Support activities can be:

- **Awareness raising, promoting services, promoting success stories**: the services offered by Chips CCs may be new and may not be well recognised in the beginning. Therefore, Chips CCs need to raise awareness about their services, need to promote their services, and may need to develop an outreach program to promote the Chips CC services to potential user companies, esp. smaller enterprises. Chips CCs may need to go to many events in their countries to increase familiarity of their services with their target customers. They may need to target specific vertical sectors. They may need to promote success stories that show how their services benefit their customers. They may need to hire staff with the right soft skills to interact with customers and provide the interface between technical Chips CC staff and customers.
- **Facilitate access to the design platform and to pilot lines** by providing information and support on how to access the platform or the pilot lines when users do not have the knowledge or expertise to do so directly.
- **Support interested users in developing semiconductor solutions (technology transfer)** by supporting technology transfer activities at local/regional/national level and – where needed – at EU level. Research activities as well as operation, administration or procurement of infrastructures are not within the scope of Chips CCs, but competence centres are expected to advise on such activities and support knowledge transfer e.g. from relevant R&I initiatives to the local semiconductor ecosystem.

Support could also be in the form of matchmaking between a research organization and a user.

- In addition, Chips CCs could grant facilitated access to experts in such areas as legal compliance and business development. They may offer assistance to SMEs in creating business plans and conducting market studies.
- **Providing (access to) training on skills**: Advanced training on specific design and manufacturing skills and practices is often difficult to access for SMEs and other stakeholders. They need access to education services for development of skills in different disciplines but also for different audiences or levels (e.g. bachelor, masters level), access to top-level teachers, or support for the set-up of a credentials/micro-credentials framework. Chips CCs should support local and national training and skills development in the area of semiconductor technologies through face-to-face as well as online training (e.g. via MOOC platforms). Chips CCs should determine what is needed in their countries, should know the competences of other Chips CCs, and – where needed – provide trainings to other CCs ('train-the-trainer'). Trainings can be provided by CCs themselves, or by third parties hired by the centres. A variety of training models can be used, ranging from alternation model or cluster model, via on-the-job trainings and apprenticeships, to crash courses and mentoring programmes.
- **Participate in the organization of a European Network of Chips Competence Centres** (**ENCCC**) **and facilitate the access to this network.** Part of the resources of a Chips CC should be dedicated to building and extending this network, in collaboration with a Coordination and Support Action (see Chips-CCC-2 : Support to the European Network of Chips Competence Centres). Chips CCs should help stakeholders, especially smaller companies such as SMEs and start-ups, to connect to other competence centres within the overall network of competence centres. They should provide stakeholders with information on relevant competences in the network as well as on national and international programs, companies, and research centres in semiconductors. A Chips CC should help a stakeholder to connect to the right competence centres within the overall network of competence centres, if the local/national Chips CC does not have the right competences to support the stakeholder. In return, a Chips CC will support stakeholders from other regions and countries that need its (specialised) expertise through the network of competence centres.
- Chips CC should act as **entry points to other European initiatives**, such as the network of European Digital Innovation Hubs, HPC competence centres, cybersecurity centres, etc. The goal is to ensure that national stakeholders have access to the best

available expertise and support in Europe, by matching stakeholders' needs with the available expertise in the network of competence centres. Such expertise may be the specialisation of another competence centre and be accessible through the ENCCC.

- **Promoting the Chips Fund and facilitating access to venture capital:** SMEs and startups are often faced with insufficient financial support and have difficulties to get loans, equity, and/or grants. In particular, startups experience difficulties in managing resources and investment at the initial stage. Competence centres in semiconductors may support SMEs, startups, and other companies to access the Chips Fund. They may also support companies in finding investors, including venture capital.
- **Awareness raising, promoting services, promoting success stories**: the services offered by Chips CCs may be new and may not be well recognised in the beginning. Therefore, Chips CCs need to raise awareness about their services, need to promote their services, and may need to develop an outreach program to promote the Chips CC services to potential user companies, esp. smaller enterprises. Chips CCs may need to go to many events in their countries to increase familiarity of their services with their target customers. They may need to target specific vertical sectors. They may need to promote success stories that show how their services benefit their customers. They may need to hire staff with the right soft skills to interact with customers and provide the interface between technical Chips CC staff and customers.

Chips CCs should primarily offer services that address the needs from their prime user communities. Nevertheless, Chips CCs should also answer the needs from other organisations, e.g. from other countries, and work in close coordination and collaboration with the rest of the Network to achieve the highest possible impact, ensure the most efficient use of the CCs' resources, and to avoid duplication of efforts among the Chips CCs and with other initiatives, such as the European Digital Innovation Hubs.

3.3.4. Access to the Chips CC

Access to a Chips CC's services shall be open to several users and be granted on an **open, transparent and non-discriminatory basis**.

In line with the Chips Act, services to SMEs or public sector organisations (e.g., RTOs) could be made available **for free or against reduced prices**, and **against market prices for large companies**. Given that large enterprises need to pay the market price, they will not be considered as beneficiaries of State aid. Conversely, public entities involved in non-economic activities or exercising public authorities' functions can benefit from access granted at reduced fees or for free, as such activities are not subject to State aid control. However, public entities

(and also research organisations) when involved in economic activities, follow the same rules as applicable to large undertakings vs SMEs, i.e. they need to pay the full market price (large undertakings) or get access at reduced fees or for free (SMEs).

As a consequence, every competence centre must, in their proposal, draw up an **indicative price list for all their services, based on market prices**. The **reduction of prices** for SMEs or other eligible entities has to be made public as well, similarly to the prices charged on market terms by the competence centres. Proposals must include the methods to calculate the market price used in the price list and/or the cost of the services, so that external experts can evaluate its validity and appropriateness.

Moreover, services provided should be accessible in the national languages as well as in English.

The Chips CCs must be established as organisations with appropriate visibility to national, regional and local communities. In general, Chips CCs should employ semiconductor specialists, primarily with full-time contracts, and with expertise in areas that are most relevant for the national communities and the specialisation of their centres. A Chips CC should have an independent organisational structure and its staff should not work under external supervision.

3.3.5. Consortia for CC

A Chips CC is a **single organisation** or a **coordinated group** of organisations (consortium) with complementary expertise, established with a **non-profit objective**, aiming to promote the use of semiconductor technologies. In the case of a consortium, one organization will be appointed as coordinator. Although there is formally no limit on the number of entities setting up a competence centre, a small number of partners per Chips CC is desirable. There is no obligation for a group of organisations to create a dedicated legal entity. A Chips CC can be built on established entities in the field or can be set up from scratch.

As a matter of example, Research and Technology Organisations (RTOs) and universities could become a national competence centre of a Participating State in semiconductors. Enterprises may also set up a competence centre, or be part of a group establishing a competence centre. However, the centre must have a non-profit objective and services must be offered not-for-profit.

Candidates for competence centres are not limited to those legal entities that are involved in the set-up of pilot lines, the design platform, or are somehow involved in any other way in the Chips for Europe Initiative. Being involved in the setup and/or operation of infrastructures is

not a requirement for competence centres. The Participating States have the sole and direct responsibility to propose candidate competence centres.

The Chips for Europe Initiative will support the establishment of competence centres **throughout the Union and Participating States**. The European Network of competence centres in semiconductors may comprise zero, one, or more centres per eligible country (Participating States). Participating States may decide to team up with other countries and support **cross-border competence centres**.

Typical **users** of the services offered by a Chips CC are companies, in particular local/national SMEs and startups, RTOs, and academic institutions at the regional, national and EU level. Public authorities and large enterprises may also use the services of a competence centre, but normally they are not the prime customers.

3.3.6. Size, funding and access to services

The call will be implemented as a single DEP call with open access. As a result of the evaluation of the call, selected consortia will be offered to sign a DEP grant.

The Union will make available **up to EUR 1 million per year, per country, for a 4-year period**. There is no differentiation based on country size, i.e. all countries may get the same maximum amount of EU funding per year to support their competence centres. There is also no differentiation based on the number of competence centres that a country wants to support, i.e. the maximum, annual amount of EU funding may be used to support one or more competence centres.

Participating States are expected to **co-finance** their national competence centres together with the Union, i.e. 50% will be funded through EU contributions and 50% through national contributions. Union funding is conditional on the availability of the same (or higher) amount of national contributions. Participating States may provide the same amount of maximum annual, financial contributions as the Union, i.e. EUR 1 million per year. Participating States may also opt to provide a higher amount of annual national contributions (i.e. higher than EUR 1 million per year), but this will not lead to a similar, higher annual Union contribution. Participating States may provide a lower amount of annual national contributions (i.e. lower than EUR 1 million per year), and this will lead to a similar, lower annual Union contribution.

The EU funding for the competence centres will be made available through Digital Europe grants, which allow to fund **specific cost items**:

- Qualified personnel of the competence centre to deliver the services mentioned above to the organisations participating in a CC, including subcontracting for specialists;

- Procurement and/or depreciation costs for equipment and facilities, both hardware and software;
- Travel grants for personnel of the competence centre and local stakeholders to carry out their activities.
- Indirect costs are included as 7% of the direct cost.

3.3.7. Type of Action

DIGITAL Simple Grants – 50% **maximum** EU funding rate.

3.3.8. Admissibility

Admissibility conditions are described in Annex II "General DIGITAL conditions" of this document.

As an additional admissibility condition, only proposals coming from a consortia of a country that had not already submitted a proposal for Call DIGITAL-Chips-2024-SG-CCC-1 will be admissible.

Regarding page limits:

- The page limit for the chapter RELEVANCE is 20 pages
- The combined page limit for the 2 chapters below is 60 pages:
  - IMPLEMENTATION.
  - WORK PLAN, WORK PACKAGES, ACTIVITES, RESOURCES ANT TIMING.
- The page limit for the chapter IMPACT is 20 pages.

3.3.9. Eligibility and selection process

Applications will only be considered eligible if their content corresponds wholly (or at least in part) to the topic description for which they are submitted.

Participant eligibility conditions are described in Annex II "General DIGITAL conditions" of this document.

Candidates to the consortium for a Chips CC must at least fulfil the following criteria:

- Appropriate competences to provide the services outlined above;
- Appropriate management capacity, staff and infrastructure necessary to provide the services outlined above;
- Operational and legal means to apply the administrative, contractual, and financial management rules that come with a grant agreement;

- Appropriate financial viability, corresponding to the level of funds they will be called upon to manage.

The Chips JU will launch an **open call for proposals** to set up competence centres in semiconductors. To be eligible, a proposal submitted to the call will have to provide proof that the centre has been designated by its Participating State and that it will be co-financed by the Participating State. In particular, **the proposal shall include as mandatory document a letter describing the formal commitment of the Participating State,** as the one provided in Annex I to the present document.

In the **evaluation phase**, the Chips Joint Undertaking will evaluate proposals by designated candidate centres. In case a Participating State has designated more candidates than its desired number and size of competence centres, the evaluation will be competitive. Otherwise, the evaluation will be a quality assessment of designated candidates.

Eligible proposals will be evaluated according to the criteria of DEP (see Award criteria) and all those scoring above all thresholds will be ranked. Based on the ranked list, the Chips JU's Public Authorities Board will select proposals for funding. Selected proposals will get a grant from the Chips JU for a duration of 4 years.

Further details on the evaluation procedure are described in the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU.[6]

3.3.10. Financial and operational capacity and exclusion

Please refer to Annex II "General DIGITAL conditions" of this document.

3.3.11. Award criteria used for open calls.

The award criteria used are as follows:

Criterion 1 - Relevance

- Alignment with the objectives and activities as described in **section 2.1 of the Chips JU Work Programme 2023-2027- Appendix 4.**
- Contribution to long-term policy objectives, relevant policies and strategies, and synergies with activities at European and national level;

6 Decision GB 2024.71

Criterion 2 - Implementation

- Maturity of the proposed CC;
- Soundness of the implementation plan and efficient use of resources;
- Capacity of the applicants, and when applicable the consortium as a whole, to carry out the proposed work.

Criterion 3 - Impact

- Extent to which the project will achieve the expected outcomes and deliverables referred to in the call for proposals and, where relevant, the plans to disseminate and communicate project achievements;
- Extent to which the project will strengthen competitiveness and bring important benefits for society;

3.3.12. Score

The scores will be given with a resolution of one decimal.

Criteria	Range	Weight (**)	Threshold (*)
Relevance	0-5	1	3
Implementation	0-5	1	3
Impact	0-5	1	3
Total	0-15		10

(*) threshold applies to unweighted score.
(**) the weight is only used to establish the ranking of the proposals.

3.4. Chips-2024-CPL-5: Pilot Line on Advanced Photonic Integrated Circuits

Chips-CPL-5	
Max EU Expenditure • Call for Expression of Interest DIGITAL-Chips-2024-CfEoI-CPL-5 • Setup, integration HORIZON-Chips-2024-RIA-CPL-5 • Operational DIGITAL-Chips-2024-SG-CPL-5	***Max. EURO 190 Mio*** ***Indicative EURO 105 Mio; Max EURO 150 Mio*** ***Indicative EURO 65 Mio; Max EURO 105 Mio*** ***Indicative EURO 20 Mio; Max EURO 40 Mio***
Mode	***Call for Pilot Line (CPL)***
Security (for DIGITAL calls only)	***Call restricted on the basis of Article 12(6) of the Regulation (EU) 2021/694***[7]
Publication date	***25th July 2024***
Deadline Submission of proposals	***17th September 2024 at 17:00 Brussels Time***

3.4.1. Context

The digital transformation and the shift towards more sustainable energy solutions have led to a profound change in the technological demands of various industries, from telecommunications to healthcare and automotive sectors. Traditional electronic circuits, primarily based on silicon, are reaching their physical and operational limits, especially in terms of efficiency, speed, and miniaturization. This challenge is magnified by the increasing complexity of applications such as 5G/6G communications, autonomous driving, and pervasive AI technologies, which demand rapid processing and transmission of vast amounts of data with minimal latency and power consumption.

Photonic Integrated Circuits (PICs), which leverage light to process and transmit information, emerge as a transformative solution to these challenges. Unlike their electronic counterparts, PICs offer the potential for higher bandwidth, faster speeds, and lower energy consumption, making them ideal for the next generation of high-performance computing systems, advanced sensor arrays, and ultra-fast communication networks. The integration of PICs with Electronic Integrated Circuits presents a compelling synergy that can address critical bottlenecks in electronic systems, particularly in data centres and cloud computing infrastructures where energy efficiency and processing speed are paramount.

Europe stands at a juncture in the field of integrated photonics. While it has established a robust foundation in photonics research and industrial applications, the region faces intense global competition, notably from North America and Asia, where significant investments are being

7 Refer to Annex IV for further information on the application of this article.

funnelled into the development of advanced PIC technologies. Europe's technological sovereignty and competitiveness in global markets increasingly hinge on its ability to innovate and maintain leadership in the emerging sector of photonic technologies.

To address these challenges and opportunities, there is a pressing need to establish a dedicated pilot line for Photonic Integrated Circuits within Europe. This initiative will focus on advancing PIC technologies beyond the current state-of-the-art, particularly extending operational wavelengths from the near-infrared into the visible and mid-infrared spectrums. This expansion is crucial for tapping into new application areas such as biomedical imaging, quantum computing, and environmental sensing, which require specific wavelengths for optimal performance.

The proposed pilot line needs to serve as a critical infrastructure for bridging the gap between laboratory research and industrial-scale production, facilitating the development of reliable, scalable, and cost-effective PIC solutions. It should foster collaboration among research institutions, SMEs, and large corporations across Europe, driving innovation, and accelerating the commercialization of PIC technologies. By doing so, it should not only enhance Europe's competitive edge in a key technological domain but also contribute significantly to the continent's economic resilience and strategic autonomy in critical technologies.

3.4.2. Expected Outcomes

The proposed pilot line shall be established with all the necessary equipment, facilities, and needs to target the following main **objectives**:

- **Develop and enhance PIC technologies** by extending the operational wavelengths into the visible and mid-infrared spectrum, crucial for applications such as lidar and advanced sensing.
- **Develop scalable and cost-effective manufacturing processes** for PICs**,** ensuring compatibility with current industrial standards and promoting widespread adoption.
- **Foster the integration of PICs** with electronic integrated circuits**,** enhancing the functionality and efficiency of combined systems for applications in computing, telecommunications, and beyond.
- **Innovate in** the fields of photonic **testing and packaging** to improve reliability, scalability, and performance of PICs.
- **Enable rapid prototyping** through Multi-Project Wafer runs**,** allowing for timely validation and iteration of PIC designs.
- **Develop demonstrators** to validate the achievement of the advanced PICs technology and to quantify its performance.

Expected Results of the Pilot Line:

The **expected results** for this pilot line should therefore comprise:

- A **sustainable pilot line open to all European stakeholders**, especially focusing on enabling SMEs and start-ups to leverage advanced PIC technologies.
- **Process Design Kits and Assembly Design Kits,** crucial for the design and development of next-generation PICs.
- Extended capabilities of current PIC technologies to **larger wafer sizes and integrate built-in self-test methodologies,** enhancing the performance and integration of PIC modules.
- Creation of **intellectual property**, boosting European production capacities in PIC technologies.
- Fostered collaborative development through **synergies with other Chips JU pilot lines**, enhancing the overall innovation capacity and technological leadership of Europe in semiconductor technologies, ensuring complementarity especially with the pilot lines dedicated to quantum technologies, heterogeneous integration, and wide bandgap materials.
- Comprehensive **training programs and skill development initiatives** to ensure that European technologists and engineers are equipped with the knowledge and tools necessary to excel in the field of photonic integration.

3.4.3. Scope

The proposed pilot line should work at all levels of the main technological steps:

- The **development of advanced PIC modules to enhance performance capabilities in existing systems** and address the high demand for faster data processing and communication. This will involve improving light source technology, detector efficiency, and modulator capabilities, particularly extending into the visible and mid-infrared spectrums. The modules will align with the latest industry standards and are expected to play a crucial role in applications ranging from telecommunications to advanced sensing and biophotonics.
- **Refinement of the fabrication processes** will be fundamental to support the production of PICs. The pilot line should optimize the lithography, etching, and deposition processes that allow for the scaling down and increased yield of photonic features.
- **Multi-Project Wafer** runs will be instrumental in the prototyping phase, offering a cost-effective route for validating and iterating PIC designs. These runs will support a variety of projects from a broad user base, including academia, research

institutions, and industry partners according to an operational and access policy defined or the collaboration with those stakeholders.

It should give open access to various PIC technology platforms, including III-V, Si, SiNx and hybrid-integration.

As part of its commitment to fostering an innovative and collaborative environment, the pilot line should **continuously deliver updated Process Design Kits** that reflect the advancements in PIC technologies. The access policy from the different stakeholders to the pilot line should be defined in the proposal according to fair and non-discriminatory principles.

The pilot line should also serve as a training ground, with the hosting entity and other partners providing necessary **training to European partners**. The training initiatives will also be directed toward students and professionals for up-skilling and re-skilling, with the goal of attracting and nurturing new talents within the European semiconductor industry.

Finally, the pilot line should promote the **collaboration** with other pilot lines, with design platforms and competence centres to enable contributions from stakeholders that develop specialized expertise in areas relevant to this pilot line's focus.

A Call for Pilot Line includes three interrelated calls:

- Call for Expression of Interest for the selection of a Hosting Consortium
- Call for proposals for Set-up, integration and process development, funded under the Horizon Europe Programme
- Call for proposals for the operational activities of the pilot line, funded under the Digital Europe Programme

The evaluation of a CPL will consist of the evaluation of the three interrelated calls.

This document describes the details of the call: topic description and the budgets as well as the procedures for evaluation and selection.

3.4.4. Specific provisions applicable to Calls for pilot lines.

The following points on access conditions, Intellectual Property, and co-ownership apply to all Calls for pilot lines. More detailed provisions are stated in the Call for Pilot Line part of this document; in case of conflicts, those provisions prevail over the provisions stated here.

3.4.4.1.Access conditions for pilot lines

Expressions of Interest submitted to the calls below need to take into account the following access conditions:

- Access to a pilot line needs to be open to a wide range of public and private users across the Union and granted on a transparent and non-discriminatory basis directly proportional to the financial contribution by the Union to the total costs of those activities.
- Access needs to be provided on market terms, or on a cost-plus-reasonable-margin basis for large undertakings, while granting preferential access or reduced prices for academic institutions, start-ups and SMEs.
- PDKs/ADKs need to be accessible for different categories of users (academia, research, industry etc.) and will be required to be available via the European virtual Design Platform.
- Access conditions for non-EU organisations need to take into account the Union's commitments to international cooperation under its strategic partnerships with like-minded countries.

Access to the pilot lines should be based on fair and non-discriminatory principles and should be limited to Participating States of the Chips JU, meaning EU Member States, EEA countries and those countries that have been associated to Horizon Europe or Digital Europe Strategic Objective 6, under which the pilot lines are funded. In determining access to the pilot lines for users established in any Participating State but controlled from third countries that are not Participating States of the Chips JU, consortia must take into consideration the following two main criteria:

- EU added value, i.e., their contribution to the objectives of the Chips Act as set out in Article 4.
- Economic security considerations.

The above access criteria should also be duly considering other relevant provisions of the Chips Act Regulation (notably Recital 11, and Recital 27), such as for example those in relation to the handling of sensitive information, potential risks of infringement of intellectual property (IP) rights, unauthorised disclosure of trade secrets and IP rights, security, confidentiality, or the leakage of sensitive emerging technologies within the semiconductor sector.

Only users from organisations that can clearly demonstrate their contribution to EU added value, their alignment with European economic security shall be granted access. Users from third countries will be granted access when this is foreseen in the international obligations of the Union concerning semiconductors, as these defined in any relevant Digital Partnerships or Trade and Technology Council agreements. In this case, such users should still commit to fulfil the above access criteria.

Selected consortia will be tasked to further elaborate on the above access criteria as well as access conditions and widely publish them. Such access conditions shall duly take into consideration the following elements: security procedures (both for physical and digital), cybersecurity protection of digital systems used to operate the pilot line, access control to facility and digital systems (including logging of access), security clearance, setup of different restricted areas with different security levels (such as the compartmentalisation of both digital and physical infrastructures).

3.4.4.2.Intellectual Property

Expressions of Interest submitted to this call need to take into account the following provisions on Intellectual Property:

- Intellectual Property provisions must comply with standard Horizon Europe and Digital Europe rules. For instance, IPR transfers to legal entities outside the EU will be subject to approval by the granting authority.
- However, any transfer of IP rights from the hosting consortium to any third parties needs to be tied to either potential investment in Europe or an international agreement.
- Possible conditions for non-exclusive licensing of IP need to be considered.
- Consortia are invited to further reflect on the impact of EU co-ownership on IP policy.

3.4.4.3.Co-ownership

The ownership share of the Chips Joint Undertaking of the acquired equipment infrastructure in a pilot line is 50%.

3.4.5. Other general provisions

1. ***Gender dimension***
   The integration of the gender dimension (sex and gender analysis) in research and innovation content is not a mandatory requirement. However, activities concerning user interaction or sensing (e.g. of medical devices, consumer goods, cars with automatic driving features, ...) need to include (if relevant) considerations of how the gender dimension affects system design, and hence whether it affects the technical specifications.

2. ***Financial capacity.***
   In line with the Financial Regulation, coordinators will be invited to complete a self-assessment using an on-line tool.

3. ***Consortium agreement:***
   Participants are required to conclude a consortium agreement. For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

4. ***Costs for the pilot line:***
   can be introduced as of the day after the publication date of the Call for Pilot Line.

3.4. Chips-2024-CDP-1: Design platform

Chips-2024-CDP-1	
Max EU Expenditure • Call for Expression of Interest DIGITAL-Chips-2024-CfEoI -CDP-1 • Coordination and Support Action DIGITAL-Chips-2024-CSA-CDP-1	***EURO 0*** ***Max. EURO 25 Mio***
Mode	***Call for Design Platform.***
Publication date	***4th Jul 2024***
Opening date	***12th Aug 2024***
Security	***Call restricted on the basis of Article 12(6) of the Regulation (EU) 2021/694[8]***
Deadline Submission of proposals	***10th Oct 2024 at 17:00 Brussels Time***

3.4.1. Context

Semiconductor circuit design is the process of creating integrated circuits (ICs) and system-on-chips (SoCs) by defining the functionalities and characteristics of chips, capturing a substantial portion of the added value within the semiconductor value chain. The trend is moving towards more complex, application-specific, highly integrated semiconductors, making cutting-edge design crucial for competitiveness and differentiation in a wide range of applications. In this context, fabless companies are well-positioned to drive technological advancements and meet the needs of diverse applications, reinforcing their pivotal role and growth in the semiconductor industry.[9]

The Chips Act underscores the strategic importance of fostering chip design growth in Europe to enhance the competitiveness of the Union's semiconductor industry. Pillar I of the Chips Act, the Chips for Europe Initiative, outlines an ambitious plan to strengthen the Union's resilience in semiconductor technologies, including promoting the growth of fabless companies focused on leading-edge technologies. This is especially pertinent given that the European share of global fabless semiconductor companies' revenues has shrunk to critically low levels (currently around 1%), highlighting the urgent need for strategic initiatives to bolster this sector and enhance Europe's competitiveness. A critical mass of fabless companies is also key to generate further demand that would justify increased investment in semiconductor manufacturing capacity in Europe.

8 Refer to Annex IV for further information on the application of this article.

9 A fabless company is a company that designs and markets hardware devices and semiconductor chips but outsources the fabrication (manufacturing) of those devices to a specialised semiconductor fabrication plant, or 'fab'.

Recognising the Union's limited fabless capacity, and the significant barriers to entry in chip design, the Design Platform shall focus on nurturing emerging companies in the sector. The Design Platform is at the heart of the Chips for Europe Initiative, it is envisaged as a key instrument to foster the development of a strong design ecosystem in the Union, by creating a pipeline of highly innovative European fabless companies, focusing particularly on the growth of start-ups and SMEs.

At the core of the design process lie a series of Electronic Design Automation (EDA) tools, Intellectual Property (IP) blocks and Process Design Kits (PDKs) including standard cell libraries. This is coupled with either on-premises or cloud-based computing resources. Each of these elements requires a separate acquisition process for the designer, often involving very significant costs and its own complex procedures.

This activity aims at building a pioneering cloud-enabled European Design Platform that will aid users, particularly start-ups and SMEs, in accessing a wide range of advanced tools, assets and services to develop their chips. The platform, by amalgamating these resources, shall support users along the innovation process, in preparation for industrial deployment. It will facilitate increased opportunities for innovation across the industry by lowering the barrier of entry for chip design in Europe, enabling both small and large entities to drive technological progress, thereby strengthening EU's position in the global semiconductor market. To this end, the Design Platform shall encompass a combination of a cloud-based infrastructure together with a number of dedicated design and other relevant services and activities, that are elaborated on further below.

The primary objectives of the platform are to cultivate a robust chip-design ecosystem in Europe and to ensure that start-ups and SMEs have access to top-tier tools and support services comparable to those more easily accessible to large enterprises. This platform, as a unified European infrastructure combined with comprehensive user support services, aims to democratise chip design in Europe by facilitating access, for all eligible users, to advanced tools and resources, irrespective of their size.

The main target users of the Design Platform shall be commercial entities, particularly start-ups and SMEs, for the purpose of pre-competitive activities such as research, development and innovation up to experimentation and tape-out. Such entities are then expected to engage in regular commercial contractual agreement with Electronic Design and Automation tool vendors outside of the Design Platform upon maturity. Complementary support to that already provided by EUROPRACTICE for academia and research institutes can be considered.

This call concerns the selection of the consortium in charge of the overall coordination of the Design Platform, referred to as the Platform Coordination Team (PCT), which shall serve as the **hosting entity** for the Design Platform's virtual infrastructure and central services, coordinating access to a wide range of tools, assets and services.

The chosen implementation model foresees a central consortium, referred to as the ***Platform Coordination Team (PCT)*** that operates the overall Design Platform initiative, serves as the hosting entity of the central cloud infrastructure and manages the development of its users. The PCT shall assist the Chips Joint Undertaking (Chips JU) in defining the technical specifications

of the cloud service for the platform to be procured by the Chips JU through a dedicated *Call for Tenders*. Following the procurement procedure, the PCT shall manage on behalf of the Chips JU the formal test, validation and delivery of the cloud-enabled platform and its integration in the broader Design Platform initiative. This shall be done in close cooperation with a selected service provider following the *Call for Tenders* for the procurement of the cloud service mentioned above. The PCT shall also be responsible for the further development and operationalisation of the Design Platform, in close cooperation with the selected service provider. It shall also be responsible for coordinating training, EDA tool and IP licensing support and the coordination of decentralised teams referred to as ***Design Enablement Teams (DETs)***. The selection of a consortium operating as the PCT is the purpose of this call.

The PCT will be complemented by a number of DETs that shall set-up a cloud-based environment for users designing on the platform, support them in their design cycle and facilitate access of users to foundry services. The PCT shall provide the set of requirements that DETs must fulfil in order to apply for integration in the cloud-based platform. A call for the DETs shall follow at a later stage.[10]

The Design Platform shall complement the ongoing EUROPRACTICE initiative, currently financed by the Chips JU project RETICLES. While EUROPRACTICE currently addresses the needs of academia, the Design Platform, in its first iterations shall target commercial enterprises, particularly start-ups and SMEs. Eventually, it is anticipated that in the future EUROPRACTICE's services may be integrated into the Design Platform.

3.4.2. Expected outcomes

The main expected outcome of this initiative is the development of a robust chip design ecosystem in Europe. Furthermore, the consortium acting in the role of the PCT is expected to contribute to the following outcomes:

- Easy cloud-enabled access to electronic design tools (including proprietary and open-source tools), libraries of design templates, as well as training and support services, available through an inclusive design platform, accelerating chip design and reducing time-to-market for users.
- The cloud services, procured by the Chips JU, may be developed and maintained by third parties, however the PCT, in line with a Hosting Agreement,[11] shall assume responsibility for the coordination and execution of the various related activities and services described below.
- The PCT shall oversee that the cloud service procured by the Chips JU is secure, scalable, and accessible 24/7. The service shall include the provision of a user help desk

10 Subject to a decision of the Governing Board of the Chips Joint Undertaking.

11 See Chapter 4.

support, robust security measures, data backup and recovery, and regular maintenance and updates.

- The PCT shall continuously monitor the operation of the Design Platform and the quality of services provided to users. This includes incorporating user feedback loops and adopting corrective measures as necessary.
- The management and maintenance of a cloud-based repository for the European chip design community, populated with an extensive portfolio of open-source and proprietary 'design assets' to facilitate and enhance the design process for users, such as intellectual property (IP) blocks, design templates, fast adoption kits, process design kits (PDKs) from pilot lines and open foundries, open-source design tools, as well as reusable open-access design elements from previous EU-funded projects.
- A quicker and more efficient licensing process for commercial EDA tools and IP libraries, reducing burden and barriers for companies engaging in chip design, coupled with a startup support programme, that includes financing of licensing costs.[12]
- Integration in the Design Platform of the design support services provided by specialised design service providers, known as Design Enablement Teams, that will be designated following a subsequent linked call.[13]
- Advanced training and support services available to a wide range of users via the Design Platform complementing the work of the network of Competence Centres and/or potential future dedicated actions on design skills to support the development of design skills across the Union.

The Design Platform is expected to support the design of a wide variety of technologies, specifically but not limited to digital circuits at multiple process nodes (up to leading edge nodes); analogue; mixed-signal; power; photonics and quantum. The Design Platform shall also support back-end of line (BEOL) design and manufacturing through advanced heterogeneous systems integration and advanced packaging techniques.

3.4.3. Scope

The purpose of this call is to select a consortium that will be responsible for implementing, hosting and running the Design Platform and coordinating its development, operation, and maintenance as well as related user support activities, in close collaboration with the Chips Joint Undertaking.

12 The scope and budget for said start-up support programme is subject to an upcoming linked call, which is subject to a decision of the Governing Board of the Chips Joint Undertaking.

13 Design Enablement Teams shall offer customised support to users throughout their entire chip development process. That will include running design tools and simulations on the cloud, design flow support and customisation, application engineering, access to Process Design Kits (PDKs) as well as prototyping and fabrication services from leading foundries and from the Chips for Europe Initiative pilot lines or other pilot lines.

To achieve those goals, proposals should address all of the following activities:

1. **Comprehensive Planning and Development**
    - Provide a comprehensive plan for the development and operation of the Design Platform, including clearly defined development and implementation targets, milestones, and key performance indicators (KPIs) for the platform's development and service delivery.
    - The PCT shall seek to establish advisory groups comprising end-user companies, potential Design Enablement Teams, and other relevant stakeholders to provide critical insights and guidance throughout the development and operationalisation of the Design Platform. These advisory groups shall be particularly pertinent prior to the potential launch of future calls concerning Design Enablement Teams and eventually, user support.
2. **Cloud service management**
    - Develop and provide detailed and comprehensive **technical specifications** for the procurement of the cloud services that will support the implementation of the envisaged Design Platform. The specifications must fulfil all the key functional requirements and objectives as herein outlined in Annex B, including the development and operational maintenance of the required infrastructure and services. These specifications shall serve as the basis for an eventual *Call for Tenders* by the Chips Joint undertaking.
    - In close coordination with the selected tenderer, **validate, test, manage and maintain** the cloud service targeted towards the European chip design community, to be gradually populated with a portfolio of open-source and proprietary 'design assets' to facilitate and enhance the design process for users, such as intellectual property (IP) blocks, design templates, fast design adoption kits, process design kits (PDKs) from pilot lines and open foundries, open-source design tools, as well as reusable open-access design elements from previous EU-funded projects.
    - Establish and maintain a rich repository of intellectual property (IP), EDA tools, and other design assets. This repository will include open-source resources as well as outputs from European projects funded under the Chips JU, its predecessors, and other sources. The aim is to provide a comprehensive, accessible, and continuously updated collection of tools and IP to support innovation and development across the platform.
3. **Complementarity to other objectives of the Chips for Europe Initiative**
    - Integrate PDKs/ADKs and services stemming from the pilot lines of the Chips for Europe Initiative into the Design Platform, in close cooperation with the pilot lines' hosting entities. This shall allow an easier and faster prototyping of designs developed using the European Design Platform on the pilot lines.

- Work closely with Competence Centres to support their users through the resources and services of the Design Platform.
- Support the design development of quantum chips, taking into consideration actions under the Chips Joint Undertaking in this area.
- Organise and provide advanced training programmes for users and developers on the platform focusing on integrated circuit design and system integration technologies, to enhance their understanding and efficient use of the provided tools and resources. Such initiatives should be undertaken in coordination with the network of Competence Centres and other skills-related initiatives of the Chips JU.

4. Technical Requirements and Standards

- Outline and provide the technical requirements, specifications, and service quality standards necessary for the selection and integration of suitable Design Enablement Teams, to ensure that the Design Platform can address the needs of its users across their chip development process, including support for prototyping and fabrication of ICs and fully packaged systems.
- Implement monitoring procedures to ensure that the central platform and the Design Enablement Teams meet the established technical standards and performance metrics. This includes regular audits and updates to the technical specifications as needed.
- Undertake continuous monitoring of the Design Platform's operations and the quality of services provided to its users. This process should include the systematic collection and analysis of user feedback to identify areas for improvement. Furthermore, appropriate corrective measures should be promptly implemented to address any identified issues, ensuring the platform maintains high standards of service and user satisfaction.

5. Supplier Negotiations and Management

- Under the direction and mandate of the Chips JU, conduct negotiations with key suppliers of Electronic Design Automation (EDA) tools and intellectual property blocks. The objective is to establish suitable master framework agreements between the Chips JU and each vendor, ensuring cost-effectiveness and securing the most favourable conditions for users of the Design Platform at various development stages.
- Manage on behalf of and under the direction of the Chips Joint Undertaking the aforementioned master framework agreements with the various vendors of EDA tools, IP libraries, and other relevant suppliers.

6. Start-up and SME support

- Provide technical and operational support to the Chips JU in the execution of calls for proposals for the selection of projects from fabless companies eligible for financial support from the Union and Participating States, which will help cover part of the costs of licensing and other operational expenses incurred during chip development.

- Ensure the provision of a dedicated 24/7 user help desk support to assist with any queries or issues related to the operation of the Design Platform.
- Run a start-up incubation and acceleration programme as set out in Annex C.

7. **Dissemination and User Engagement**

- Effectively disseminate to potential users, start-ups and SMEs, the services offered via the Design Platform. Dissemination should also be carried out through the Network of Competence Centres of the Chips for Europe Initiative.

The above shall be considered in proposals in light of the access conditions set-out in section 2.4.5.

In addition to the activities defined above, the PCT Consortium should also provide advisory services to potential users of the Design Platform, guiding them on how to fully leverage the opportunities provided by the platform. This includes detailed assistance during the initial onboarding process to ensure users are effectively integrated and can navigate the platform's resources with ease. Successful applicants shall convincingly demonstrate their competence and capabilities to establish a Design Platform with all the necessary infrastructure, governance, and access facilities to execute the above stated activities.

Fabless semiconductor companies, especially startups and SMEs are the primary target groups of the proposed activities and as such they are not expected to participate directly in the PCT consortium, but they should be supported by activities funded by this call. Therefore, the PCT consortium is to be formed mostly by entities that can operate without conflicts of interest, such as academic institutions and research and technology organisations with a strong track record in IC design, chip design enablement and related activities.

The PCT consortium should implement robust governance policies that enforce openness, transparency, impartiality, including a diverse representation from across the industry. The diversity of tools offered on the platform should foster competition among software providers and avoid vendor lock-in. The goal is to create a level playing field where European fabless semiconductor startups and SMEs can benefit from a collaborative environment that supports pre-commercial innovation, competition, and fair market practices. During the implementation of the Design Platform, the consortium shall follow the policy steering provided by the Chips JU.

It is expected that the project will have a duration of at least three years.

A Call for Design Platform (CDP) includes two interrelated calls:

- Call for Expression of Interest for the selection of a Hosting Consortium,
- Call for Proposals for coordination of the Design Platform funded under the Digital Europe Programme (DEP). The type of action is a Coordination and Support Action (CSA).

In practice, this means that **applicant consortia will have to submit proposals** for each of the abovementioned calls. Each call will have its specific evaluation criteria.

The document describes the details of the CDP, including topic description and budgets as well as the procedures for evaluation and selection.

The overall development of the Design Platform can be outlined in four high-level stages, with the main milestones as follows:[14]

- Phase 1: The selection of the consortium in charge of the overall coordination of the Design Platform, referred to as ***the Platform Coordination Team*** (PCT); the definition of technical specifications for the procurement of the cloud service and call for Design Enablement Teams (DETs), and the launch of the project.
- Phase 2: Following the definition of the relevant technical specifications in Phase 1, launch of the procurement process for the cloud service and the call for DETs.
- Phase 3: Integration of all components i.e. cloud service, design assets, DETs and other relevant elements and the operationalisation of the platform. Formal launch of the platform, with availability of the cloud service on a 24/7 basis.
- Phase 4: The potential launch of a scheme to support start-ups and SMEs making use of the Platform.[15]

3.4.4. Type of Action

Reimbursement rate as percentages of the eligible costs

- EU contribution as % of the eligible cost according to Digital Europe (*): up to 100%

(*) beneficiaries may ask for a lower contribution.

3.4.5. Specific Provisions applicable to the Call for Design Platform

The following points on access conditions apply to the Call for Design Platform. Interested consortia should read this section in tandem with the rest of the work programme text on the Design Platform, particularly the technical description in section 2.4; in case of conflicts, those provisions prevail over the provisions stated here.

3.4.5.1.Services

In line with the technical description provided in Section 2.4, the Design Platform, particularly the PCT Consortium, shall provide two classes of services.

14 The different phases of development are indicative. Consortia may propose justified deviations to this plan. Phases are not necessarily sequential and may be run in parallel.

15 Subject to a decision of the Governing Board of the Chips Joint Undertaking.

The **first level of services** shall be the base level of services open to a wide range of users that fulfil the access conditions set out below in this section. When it comes to first level services, consortia seeking to assume the role of PCT as per the technical specifications in Section 2.4 are expected to provide at least the following services:

- A startup support programme, including incubation and mentoring activities.
- Advanced training sessions and support services available through the Design Platform. Activities to improve chip design skills across the Union such as tutorials, workshops, and personalised support, working in liaison with the Competence Centres and other dedicated initiatives across the Union.
- Access to a comprehensive cloud-based repository, as per the procured cloud service by the Chips JU and the hosting agreement. This repository shall contain essential design resources, including intellectual property (IP) blocks, design templates, fast adoption kits, and process design kits (PDKs) from pilot lines and open foundries, open-source design tools and reusable design elements, including from previous EU-funded projects.
- Access to PDKs/ADKs from state-of-the-art Chips for Europe Initiative pilot lines and to open-source foundry PDKs/ADKs.
- Facilitate access to services provided by the Chips for Europe Initiative pilot lines through synergies with their hosting consortia.
- A sandboxing environment for open-source Electronic Design Automation (EDA) tools and intellectual property (IP). An exchange for chip designs in a secure environment, enabling users to share insights and developments with the broader Design Platform community.
- A streamlined licensing process for commercial EDA tools and IP libraries. Overcome traditional barriers and reduce the administrative burden associated with licensing, facilitating easier and faster engagement in chip design activities.

The **second level of services** shall be primarily targeted towards selected start-ups and SMEs receiving support from public authorities. When it comes to second level services, consortia answering to this call are expected to provide, but are not limited to, the following:

- A startup support programme, including acceleration and mentoring activities. This may potentially be complemented by a financing support scheme.[16]

16 The scope and budget for said start-up support programme shall be subject to a decision by the Governing Board of the Chips Joint Undertaking.

- A coordinated and rich network of Design Enablement Teams (DETs) as set out in Annex A covering a wide range of technologies.

- Technical and commercial mentoring to start-ups and SMEs in the support programme, with technical support being primarily the remit of DETs.

- Access, via DETs, to application engineering support and a wide variety of foundries and pilot lines for prototyping, Multi-Project Wafer (MPW) service and eventual tape-out.

- Access to a commercial and open-source IP repository for prototyping of chips.

- Access via a DET of choice to a customised cloud instance with the appropriate design flow and scalable computing and storage resources.

Users without public financial support may still access all the above services at market rates. The PCT shall serve as a non-profit and strive to ensure favourable pricing through for example efficiencies of scale.

3.4.5.2.Access Conditions

The following general principles apply to the access-to-use of the Chips for Europe Initiative's infrastructures including the Design Platform:

- Access should be made **available to a wide range of users across the Union** as per specific conditions set-out below;[17]

- Access should be granted on a **transparent** basis, i.e. information regarding the criteria, processes, and terms governing access to the infrastructures should be clear and transparent to ensure that potential users have a comprehensive understanding of the access framework;[18]

- Access should be granted on a **non-discriminatory** basis, i.e. preferential treatment of potential users based on their geographic location in the Union, affiliation, etc. should be avoided; [19]

- Access by EU users, i.e. users established in the Union, should be (at least) directly **proportional to the financial contribution by the Union** to the total costs of those activities; [20]

17 Council Regulation (EU) 2023/1782 Article 128(5)

18 Council Regulation (EU) 2023/1782 Article 128(5)

19 Council Regulation (EU) 2023/1782 Article 128(5)

20 Council Regulation (EU) 2023/1782 Article 128(5)

- Access needs to be provided on transparent **market terms**, or on a cost-plus-reasonable-margin basis for large undertakings, while granting **preferential access or reduced prices** for academic institutions, start-ups and SMEs. In case of reduced prices, price differences must be monitored by the hosting consortium; [21]

- Access should be granted to **international research and commercial partners**, if this is foreseen in Digital Partnerships and Trade and Technology Councils of the Union as part of its agreement with its international strategic partners.[22]

- In case of **excessive demand** for access to an infrastructure, responsible organisations, in this case the PCT consortium, need to put in place mechanisms to ensure fairness, transparency, and equal opportunity for all interested parties;

3.4.5.3.EU added value and economic security considerations

Access to the Design Platform should be based on fair and non-discriminatory principles and should be limited to Participating States of the Chips JU, meaning EU Member States, EEA countries and those countries that have been associated to Horizon Europe or Digital Europe Strategic Objective 6, under which the design platform is funded. In determining access to the Design Platform for users established in any Participating State but controlled from third countries that are not Participating States of the Chips JU, consortia must take into consideration the following two main criteria:

- EU added value, i.e., their contribution to the objectives of the Chips Act as set out in Article 4.
- Economic security considerations.

The above access criteria should also be duly considering other relevant provisions of the Chips Act Regulation (notably Recital 11, and Recital 27, such as for example those in relation to the handling of sensitive information, potential risks of infringement of intellectual property (IP) rights, unauthorised disclosure of trade secrets and IP rights, security, confidentiality, or the leakage of sensitive emerging technologies within the semiconductor sector.

Only users from organisations that can clearly demonstrate their contribution to EU added value, their alignment with European economic security shall be granted access. Users from third countries will be granted access when this is foreseen in the international obligations of the Union concerning semiconductors, as these defined in any relevant Digital Partnerships or Trade and Technology Council agreements. In this case, such users should still commit to fulfil the above access criteria.

Selected consortia will be tasked to further elaborate on the above access criteria as well as access conditions and widely publish them. Such access conditions shall duly take into

21 Council Regulation (EU) 2023/1782 Recital 9 & Regulation (EU) 2023/1781 Recital 18

22 Regulation (EU) 2023/1781 Recital 18

consideration the following elements: security procedures (both for physical and digital), cybersecurity protection of digital systems used to operate the Design Platform, access control to facility and digital systems (including logging of access), security clearance, setup of different restricted areas with different security levels (such as the compartmentalisation of both digital and physical infrastructures).

3.4.5.4.Specific Access Provisions

Furthermore, specifically when it comes to Level 1 services:

- These services should be open to all users in the EU who satisfy some basic eligibility criteria to be proposed by the applying PCT consortia. Level 1 services should be accessible to all legal entities from Chips JU Participating States against market terms with highly reduced or zero prices and preferential access for start-ups and SMEs. For those legal entities established in Participating States but controlled from third countries, the access conditions are subject to the conditions described above.

Furthermore, specifically when it comes to Level 2 services:

- In addition to access to Level 2 services via potential financial support from the Union and Participating States, companies may get access to these services via market prices. Such access follows the general principles set out above. Access for legal entities established in Participating States but controlled from third countries shall be determined based on EU added value and economic security terms as described above.
- Companies could potentially get access to Level 2 services via potential financial support from the Union and Participating States. Any potential competitive funding scheme shall include EU added value and economic security considerations as an evaluation criterion.[23]

3.4.6. Other general Provisions

1. **Gender dimension:** The integration of the gender dimension (sex and gender analysis) in research and innovation content is not a mandatory requirement. However, activities concerning user interaction or sensing (e.g. of medical devices, consumer goods, cars with automatic driving features, ...) need to include (if relevant) considerations of how the gender dimension affects system design, and hence whether it affects the technical specifications.
2. **Financial capacity:** In line with the Financial Regulation, coordinators will be invited to complete a self-assessment using an online tool.
3. **Consortium agreement**: Participants are required to conclude a consortium agreement.

23 Subject to a decision of the Governing Board of the Chips Joint Undertaking.

4. *Given the illegal invasion of Ukraine by Russia and the involvement of Belarus, there is currently no appropriate context allowing the implementation of the actions foreseen in this programme with legal entities established in Russia, Belarus, or* in non-government-controlled territories of Ukraine. Therefore, such legal entities are not eligible to participate in any capacity. Exceptions may be granted on a case-by-case basis for justified reasons. This criterion also applies in cases where the action involves financial support given by grant beneficiaries to third parties established in Russia, Belarus or in non-government-controlled territories of Ukraine (in accordance with Article 204 of the Financial Regulation No 2018/1046).

State aid: Any support provided to users of the Design Platform shall comply with European State aid rules. To this end the selected consortium shall maintain a thorough price list of all services for the purposes of monitoring the value of potential in-kind or discounted support granted to users. Start-ups and SMEs may benefit from exemptions under the General Block Exemption Regulation (GBER)[24] and/or the State aid Framework for Research and Development and Innovation (RDIF) when utilising the services offered by the Design Platform. [25]

24 Commission Regulation (EU) No 651/2014 of 17 June 2014 declaring certain categories of aid compatible with the internal market in application of Articles 107 and 108 of the Treaty on the Functioning of the European Union

25 Communication from the Commission Framework for State aid for research and development and innovation 2022/C 414/01

Call for Quantum Pilot Lines

The calls for quantum pilot lines are part of the Chips for Europe Initiative, focusing on building capacities for the accelerated development of Quantum chips. The overarching goal is to accelerate the industrialization process of quantum pilot lines and reduce time-to-market, thereby enhancing the competitive edge of the European quantum ecosystem. The objective of these calls is to launch actions for those more mature quantum chips production approaches that are close to established manufacturing processes. These more mature technologies are pivotal in advancing computing, secure communications, sensing and various other sectors, and require stabilization of their production, integrating advanced Quantum Process Design Kits (PDKs) into the European virtual design platform.

In this context, these calls will serve as a vital resource for both industry and academia, facilitating the design, processing, and validation of quantum components, systems, and applications, leveraging state-of-the-art quantum technologies. The actions launched under these calls are critical for transitioning from research to scalable industrial production, ensuring the EU's prominence as a global quantum hub.

The whole initiative to industrialize quantum pilot lines in the EU will be implemented in several phases, where the current call marks the beginning of the first phase. The subsequent phase will be supported by a budget commensurate to its level of ambition in function of the progress made during the first phase, and commensurate with the objectives to be achieved.

Proposers are invited to contact their national funding agencies for information regarding the national co-funding.

3.5. Chips-QAC-1: Call for establishing Framework Partnership Agreements for developing Quantum Chip Technology for stability Pilots.

Chips-2024-QAC-1	
Max EU Expenditure • Framework Partnership Agreement HORIZON-JU-Chips-2024-FPA-QAC-1	***Max. EURO 0 Mio funding in total.*** [26]
EU Funding rate (for SGAs)	***50%***
Mode	***Framework Partnership Agreement (FPA)***
Publication date	***5th September 2024***
Opening date	***24th September 2024***
Security	***Call restricted on the basis of Article 22(5) of the Regulation (EU) 2021/695***[27]
Deadline Submission of proposals	***21st January 2025 at 17:00 Brussels Time***

3.5.1. Context

Europe's strategic agenda to lead in the field of quantum technologies by 2030 requires a concerted effort to develop advanced quantum chips including Quantum Processing Units (QPUs). This call seeks proposals for the development of new pilot lines capable of producing quantum chips, or the adaptation and expansion of existing pilot lines in view of producing quantum chips.

The stability pilot lines should focus on achieving higher Technology Readiness Level (TRL) / Manufacturing Readiness Level (MRL) by advancing manufacturing and integration techniques tailored to meet the needs of the quantum industry over the next decade. The testing and experimentation facilities should be fully integrated in the pilot lines, providing seamless production and testing services.

Proposals are invited for pilot lines that address the production of any type of quantum chips for quantum sensing, quantum communication and quantum computing. Proposals should

26 Proposals are expected to indicate an overall budget for the implementation of a full FPA via multiple SGAs. In case of sufficient high-quality proposals submitted and evaluated, at least 2 FPA proposals are expected to be selected. The JU estimates that an EU contribution of between EUR 20 and 25 million for a first SGA, per selected FPA, would allow starting the expected outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of an FPA proposal indicating different amounts for a first SGA.

27 Regulation (EU) 2021/695 of the European Parliament and of the Council of 28 April 2021 establishing Horizon Europe – the Framework Programme for Research and Innovation, laying down its rules for participation and dissemination, and repealing Regulations (EU) No 1290/2013 and (EU) No 1291/2013. Article 22(5)

target the more mature quantum technologies like superconducting, photonic, semiconducting, diamond-based, or neutral atoms. Proposals should focus on robust, scalable quantum processing platforms that pave the way for the industrialization of the production of quantum chips and the commercialization of quantum chips. To achieve a diversified portfolio, no more than one pilot line per technology will be funded.

3.5.2. Expected Outcomes

- At least two pilot lines for quantum chips, resulting in enhanced infrastructure capable of high-yield production of quantum chips, integrating various technologies.
- Sustainable pilot lines open to European stakeholders, including SMEs and start-ups, across the whole value chain, from materials to applications, enabling technologies, and thereby creating a community of interest for those technologies.
- Advanced manufacturing techniques and integration processes tailored to the needs of the quantum industry, aiming for significant improvements in production stability and yield rates, contributing to a more reliable supply chain for quantum chips in Europe.
- A sustainable and open-access pilot line framework, significantly boosting the innovation capacity in quantum chip technologies and providing a competitive advantage to the European ecosystem.
- Enhanced collaboration and innovation within the European quantum ecosystem, fostering long-term growth and development in the sector.
- Demonstrated ability to transition from pilot production to industrial-scale manufacturing, ensuring the commercial viability of new quantum technologies.

The pilot lines can be physically located at one or distributed over several hosting sites. A hosting site is the physical facility at which a hosting entity will host a pilot line and which is established in a Participating State that is a Member State. Proposals shall include the members that will host and develop the pilot lines for the whole duration of the SGAs.

Collaborative efforts should be clearly outlined, demonstrating how the pilot lines will build on European quantum initiatives and contribute to the broader quantum technology ecosystem. This includes synergies and cooperation with the experimental pilot lines QU-PILOT and QU-TEST of the Quantum Flagship Initiative, for R&D support, and leveraging competencies across Europe to enhance the pilot lines' capabilities and outputs.

Proposals should exhibit a robust collaboration framework that integrates efforts across academia, industry including SMEs and start-ups, and existing quantum initiatives. Successful consortia should look for collaborations and synergies with other quantum technology projects and pilot lines. Consortia should promote the reusability of developed enabling technologies and methods, enhance the scalability of solutions, and foster a cohesive and innovative quantum technology landscape across Europe.

The pilot lines should aim to significantly accelerate industrialization and time-to-market resulting in a competitive advantage for the European quantum chips ecosystem. Proposals should also develop concrete industrialization plans, providing a roadmap for the transfer of elements or all of the process technology to industrial partners in their deployment of mass-production facilities.

Proposals should include for the FPA an overall plan for the development of this pilot line subdivided in phases and explaining for each phase the objectives, expected results, the needs in terms of equipment, estimates of required person months.

Proposals should clearly highlight important milestones and identify quantum specific, and ambitious KPIs (e.g. yield, quality of the quantum chips, reliability, reproducibility, high performance, and scalability of the production, etc...) that shall be met during the implementation of the pilot line. Technology and manufacturing process risk management plans for realistic and time-bound implementation should be also included in the proposals.

3.5.3. Scope

The aim is to support two or more pilot lines implemented through a Framework Partnership Agreement establishing a stable and structured long term partnerships between the Chips JU and consortia of industry, research organisations and the institutions in quantum technologies who commit themselves to establishing, coordinating and implementing a strategic and ambitious R&I initiative for the development of innovative quantum chips, followed by an ambitious action for building and deploying pilot lines.

The partnerships will be set up through one FPA per technology platform, which will ensure the implementation of the initiative through several consecutive Specific Grant Agreements (SGAs) that will carry out the different activities in a common framework. The SGAs will be implemented as Research and Innovation Actions (RIA) or Innovation Actions (IA) in function of the concrete objectives of the action. The FPAs should be carried out in different phases, which will be triggered after the attainment of appropriate intermediate progress milestones identified by the consortia. The FPAs will permit the coordinated development of the technology, its validation and the nurturing of the ecosystem. The developments should be integrated in one pilot demonstrator per FPA to validate the developments and demonstrate the scalability potential.

The infrastructures of the pilot lines should be installed in a pre-operational environment in the facilities of the hosting entities. The FPAs and SGAs should target delivering components for building and deploying in the EU of quantum technologies based on European technology.

The FPAs are expected to pursue an inclusive approach in the development of the necessary EU-wide quantum ecosystem, ensuring European wide participation of relevant stakeholders across the EU and take-up of the technology developed.

The FPAs should include research institutes, universities, RTOs, industry, including SMEs as well as any other organization that can play a role in the realization of the objectives of the initiative.

The FPAs should describe the planned mechanisms guaranteeing that all IP generated in the initiative stays in the EU and will not be transferred to third countries, dedicating an appropriate effort to IP management, protection and exploitation (i.e. IP licensing, IP warranty, etc.).

The FPAs should present a professional project structure management, a strategic R&I roadmap to implement the activities, and governance that are appropriate to coordinate the implementation of the future SGAs, including addressing the industrial use cases, and to deliver effectively and efficiently the main results of the initiative.

The FPAs should put in place appropriate management and progress control mechanisms, in particular, the establishment milestones for the SGAs assess the correct advancement of the work towards the goals of the overall initiative.

The FPAs should establish interaction with the relevant stakeholders and pilot lines and the design platform of the Chips JU to coordinate work on horizontal issues and exploit synergies where relevant.

The FPAs are expected to achieve Technology Readiness Level (TRL) 8. The actions implemented under the first SGA are expected to achieve Technology Readiness Level (TRL) 6.

Proposals should address the following activities:

- Developing scalable production processes for quantum chips in view of building industrial production processes.
- Integrating cutting-edge Quantum Process Design Kits (PDKs) with European virtual design platforms to standardize production and reduce the need for custom developments.
- Enhancing technology (including enabling technologies) and manufacturing readiness levels across the quantum industry, addressing applications in one or more of the following: quantum computing, communications, simulation, and/or sensing.
- Establishing standardized methodologies for the design, test, and manufacturing of quantum chips to streamline production processes and broaden the application sectors.
- Demonstration of scalable, efficient, and stable production capabilities, aiming at high yield[28]. The development of robust and repeatable manufacturing processes tailored to quantum chips' unique requirements, enabling a consistent and reliable supply for European stakeholders.
- Developing reliable characterization tools to ensure quality assurance of quantum chips, ensuring consistency and reliability across production batches, and demonstrating the scalability of pilot line technologies from small-to-mid volume fabrication to potentially large-scale industrial production.
- Define a technology roadmap and implementation plan towards industrialisation of the production of quantum chips.

28 Yield is defined here as the proportion of functional components to defective components within the same production run.

3.5.4. Eligibility

In order to achieve the expected outcomes, and safeguard the Union's strategic assets, interests, autonomy, and security, it is important to avoid a situation of technological dependency on a non-EU source, in a global context that requires the EU to take action to build on its strengths, and to carefully assess and address any strategic weaknesses, vulnerabilities and high-risk dependencies which put at risk the attainment of its ambitions. For this reason, participation is limited to legal entities established in Member States, Iceland, Norway and the following additional associated country: Israel.[29]

For the duly justified and exceptional reasons listed in the previous paragraph, in order to guarantee the protection of the strategic interests of the Union and its Member States, entities established in an eligible country listed above, but which are directly or indirectly controlled by a non-eligible country or by a non-eligible country entity, may not participate in the action unless it can be demonstrated, by means of guarantees provided by their eligible country of establishment, that their participation to the action would not negatively impact the Union's strategic, assets, interests, autonomy, or security.[30]

3.5.5. STEP and Sovereignty Seal

This topic contributes to the objectives of the *Strategic Technologies for Europe Platform* (STEP). As such, eligible proposals that exceed the evaluation thresholds will be awarded a *Sovereignty Seal*. The Sovereignty Seal is a quality label, valid for the duration of the project,

29 Legal entities established in Israel are eligible to participate in this action on the basis that (i) Israel is an associated country (and continues to be on the date of the opening of this topic for submission); and (ii) Israel meets specific conditions. Prior to the adoption of this Work Programme, questionnaires were sent to non-EEA associated countries and countries in the process of association in order to assess their eligibility to participate.

30 The guarantees shall in particular substantiate that, for the purpose of the action, measures are in place to ensure that:

a) control over the applicant legal entity is not exercised in a manner that retrains or restricts its ability to carry out the action and to deliver results, that imposes restrictions concerning its infrastructure, facilities, assets, resources, intellectual property or know-how needed for the purpose of the action, or that undermines its capabilities and standards necessary to carry out the action;

b) access by a non-eligible country or by a non-eligible country entity to sensitive information relating to the action is prevented; and the employees or other persons involved in the action have a national security clearance issued by an eligible country, where appropriate;

c) ownership of the intellectual property arising from, and the results of, the action remain within the recipient during and after completion of the action, are not subject to control or restrictions by noneligible countries or non-eligible country entity, and are not exported outside the eligible countries, nor is access to them from outside the eligible countries granted, without the approval of the eligible country in which the legal entity is established.

which will facilitate access to additional EU funding (alternative, cumulative or combined funding from several EU budget instruments) or national public and private investments.

3.5.6. Specific provisions applicable to this Call

The following points on access conditions apply.

3.5.6.1. Access conditions for pilot lines

Access to the pilot lines should be based on fair and non-discriminatory principles and should be limited to Participating States of the Chips JU, meaning EU MS, EEAs and those countries that have been associated to Horizon Europe, under which the pilot lines are funded. In determining access to the pilot lines for users established in any Participating State but controlled from third countries that are not Participating States of the Chips JU, the consortium must take into consideration the following two main criteria:

1. EU added value, i.e., their contribution to the objectives of the Chips Act as set out in Article 4.

2. Economic security considerations.

The above access criteria should also be duly considering other relevant provisions of the Chips Act Regulation (notably Recital 11[31], and Recital 27[32], such as for example those in relation to

31 It is a clear objective of the Union to promote international cooperation and knowledge exchange on the basis of the Union's interests, mutual benefits, international commitments, and, to the extent possible, reciprocity. Nevertheless, the infringement of intellectual property (IP) rights, the unauthorised disclosure of trade secrets, or the leakage of sensitive emerging technologies in the semiconductor sector could compromise the interests of the security of the Union. Against this background, the Commission is exploring concrete proposals to strengthen the Union's investment and export control frameworks. In addition, the Union and the Member States should cooperate with strategic partners to strengthen the joint technological and industrial leadership in accordance with applicable procedural requirements.

32 R&D within the Union is increasingly exposed to practices aiming to misappropriate confidential information, trade secrets, and protected data, such as IP theft, forced technology transfers and economic espionage. In order to prevent adverse impacts on the interests of the Union and the objectives of the Initiative, it is necessary to adopt an approach to ensure that the access to and use of sensitive information or results, including data and know-how, security and transfer of ownership of results as well as content protected by IP rights generated in connection to or as a result of actions supported by the Initiative, are protected. To ensure that protection, any actions supported by the Initiative and funded by Horizon Europe and the Digital Europe Programme should follow the relevant provisions of those Programmes, such as on participation of entities established in third countries associated with the programme, grant agreements, ownership and protection, security, exploitation and dissemination, transfer and licensing and access rights. It is possible to set specific provisions when

the handling of sensitive information, potential risks of infringement of intellectual property (IP) rights, unauthorised disclosure of trade secrets and IP rights, security, confidentiality, or the leakage of sensitive emerging technologies within the semiconductor sector.

Only users from organisations that can clearly demonstrate their contribution to EU added value, their alignment with European economic security shall be granted access. Users from third countries will be granted access when this is foreseen in the international obligations of the Union concerning semiconductors, as these defined in any relevant Digital Partnerships or Trade and Technology Council agreements. In this case, such users should still commit to fulfil the above access criteria.

In close collaboration with the Commission, the selected consortia will be tasked to further elaborate on the above access criteria as well as access conditions and widely publish them.

3.5.7. Other general provisions

1. ***Gender dimension***
   The integration of the gender dimension (sex and gender analysis) in research and innovation content is not a mandatory requirement. However, activities concerning user interaction or sensing (e.g. of medical devices, consumer goods, cars with automatic driving features, ...) need to include (if relevant) considerations of how the gender dimension affects system design, and hence whether it affects the technical specifications.

2. ***Financial capacity.***
   In line with the Financial Regulation, coordinators will be invited to complete a self-assessment using an on-line tool.

3. ***Consortium agreement:***
   Participants are required to conclude a consortium agreement. For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

implementing those Programmes, in particular with regard to limitations to transfers and licensing in accordance with Article 40(4) of Regulation (EU) 2021/695, and limitation of participation of legal entities established in specified associated or other third countries due to reasons based on the Union's and the Member States' strategic assets, interests, autonomy or security, in accordance with Article 22(5) of Regulation (EU) 2021/695 and Article 12(6) of Regulation (EU) 2021/694. Additionally, the handling of sensitive information, security, confidentiality, protection of trade secrets and IP rights should be governed by Union law, including Directives (EU) 2016/943 (11) and 2004/48/EC ( ) of the European Parliament and of the Council, and national law. It is possible for the Commission and the Member States to protect technology transfers for reasons related to Union and national security interests in relation to investments made in facilities falling within the scope of this Regulation in accordance with Regulation (EU) 2019/452 of the European Parliament and of the Council (12 13).

3.6. Chips-QAC-2: Call for establishing Framework Partnership Agreement(s) for developing Quantum Chip Technology for high-quality Trapped Ions Pilots.

Chips-2024-QAC-2	
Max EU Expenditure • Framework Partnership Agreement HORIZON-JU-Chips-2024-FPA-QAC-2	***Max. EURO 0 Mio funding in total.*** [33]
EU funding rate (for SGAs)	***50%***
Mode	***Framework Partnership Agreement (FPA)***
Publication date	***5th September 2024***
Opening date	***24th September 2024***
Security	***Call restricted on the basis of Article 22(5) of the Regulation (EU) 2021/695***[34]
Deadline Submission of proposals	***21st January 2025 at 17:00 Brussels Time***

3.6.1. Context

The ambition to position Europe as a leader in quantum technologies hinges on developing high-quality, scalable quantum chip technologies. Trapped ions represent a promising avenue, yet Europe faces challenges, notably the migration of semiconductor fabrication expertise outside the EU, reducing local knowledge and increasing dependence on non-European economies. This call seeks to develop chip-based ion-trap technologies within Europe, leveraging European designs and fabrication capabilities to ensure sovereignty and lead in ion-trap quantum technologies.

3.6.2. Expected outcomes.

- Scalable, efficient, and integrated production capacities for Europe, enhancing the availability of quantum technologies for computing, communication, and sensing.
- Sustainable pilot line open to European stakeholders (especially for SMEs and start-ups) across the whole value chain, from materials to applications, enabling

33 Proposals are expected to indicate an overall budget for the implementation of a full FPA via multiple SGAs. At most 1 FPA proposal is expected to be selected. The JU estimates that an EU contribution of up to EUR 15 million for a first SGA would allow starting the expected outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of an FPA proposal indicating different amounts for a first SGA.

34 Regulation (EU) 2021/695 of the European Parliament and of the Council of 28 April 2021 establishing Horizon Europe – the Framework Programme for Research and Innovation, laying down its rules for participation and dissemination, and repealing Regulations (EU) No 1290/2013 and (EU) No 1291/2013. Article 22(5)

technologies, and thereby creating a community of interest for those technologies, boosting the use of those technologies in Europe. The pilot line should significantly boost the innovation capacity on trapped-ion chips resulting in a competitive advantage for the European ecosystem.

- Development of a European supply chain for quantum technologies, fostering innovation capacities in SMEs and ensuring critical intellectual property remains within the EU.
- Demonstration of high-quality production with a focus on maturing the production towards scalability, efficiency, and integration of Quantum PDKs.

The pilot lines can be physically located at one or distributed over several hosting sites. A hosting site is the physical facility at which a hosting entity will host a pilot line and which is established in a Participating State that is a Member State. Proposals shall include the members that will host and develop the pilot lines for the whole duration of the SGAs.

The pilot line should aim to significantly accelerate industrialization and time-to-market resulting in a competitive advantage for the European trapped-ion chips ecosystem. Proposals should also develop concrete industrialization plans, providing a roadmap for the transfer of elements or all of the process technology to industrial partners in their deployment of mass-production facilities.

Proposals should clearly highlight important milestones and identify trapped-ion specific, and ambitious KPIs (e.g. high yield, high-quality quantum chips, reliability, reproducibility, high performance, and scalability of the production, etc.) that shall be met during the implementation of the pilot line. Technology and manufacturing process risk management plans for realistic and time-bound implementation should be also included in the proposals.

3.6.3. Collaborations

Proposals should clearly outline collaborative efforts that integrate the trapped ion pilot lines with existing European quantum initiatives, contributing significantly to the broader quantum technology ecosystem.

Proposals should provide a robust collaboration framework that integrates efforts across academia, industry, and existing quantum initiatives. Successful consortia should look for collaborations and synergies with other quantum technology projects and pilot lines. Consortia should promote the reusability of developed enabling technologies and methods, enhance the scalability of solutions, and foster a cohesive and innovative quantum technology landscape across Europe.

3.6.4. Scope

This call aims to develop a scalable production infrastructure for trapped-ion quantum computing processors in Europe, transitioning from manually fabricated ion traps to automated manufacturing processes.

The aim is to support one pilot line implemented through a Framework Partnership Agreement establishing a stable and structured long term partnerships between the Chips JU and consortia of industry, research organisations and the institutions in Quantum Technologies who commit themselves to establishing, coordinating and implementing a strategic and ambitious R&I initiative contributing to the development of innovative quantum chips, followed by an ambitious action for building and deploying pilot lines.

The partnership will ensure the implementation of the initiative through several consecutive Specific Grant Agreements (SGAs) that will carry out the different activities in a common framework. The SGAs will be implemented as Research and Innovation Actions (RIA) or Innovation Actions (IA) in function of the concrete objectives of the action. The FPA should be carried out in different phases, which will be triggered after the attainment of appropriate intermediate progress milestones identified by the Consortia. The FPA will permit the coordinated development of the technology, its validation and the nurturing of the ecosystem. The developments should be integrated in at least one pilot demonstrator to validate the developments and demonstrate the scalability potential.

The infrastructures of the pilot line should be installed in a pre-operational environment in the facilities of the hosting entities. The FPA and SGAs should target delivering components for building and deploying in the EU of quantum technologies based on European technology.

The FPA is expected to pursue an inclusive approach in the development of the necessary EU-wide quantum ecosystem, ensuring European wide participation of relevant stakeholders across the EU and take-up of the technology developed.

The FPA should include research institutes, universities, RTOs, industry, including SMEs as well as any other organization that can play a role in the realization of the objectives of the initiative.

The FPA should describe the planned mechanisms guaranteeing that all IP generated in the initiative stays in the EU and will not be transferred to third countries, dedicating an appropriate effort to IP management, protection and exploitation (i.e., IP licensing, IP warranty, etc.).

The FPA should present a professional project structure management, a strategic R&I roadmap to implement the activities, and governance that are appropriate to coordinate the implementation of the future SGAs, including addressing the industrial use cases, and to deliver effectively and efficiently the main results of the initiative.

The FPA should put in place appropriate management and progress control mechanisms, in particular, the establishment milestones for the SGAs and an intermediate main assessment point to assess the correct advancement of the different work lines towards the goals of the overall initiative.

The FPA should establish interaction with the relevant stakeholders and pilot lines, design platform, competence centres of the Chips JU to coordinate work on horizontal issues common to both communities and exploit synergies where relevant.

The FPA is expected to achieve Technology Readiness Level (TRL) 8. The actions implemented under the first SGA are expected to achieve Technology Readiness Level (TRL) 6.

Proposals should address the following activities:

- Integrating fabrication capabilities into mainstream microelectronics or photonics manufacturing processes.
- Microfabrication techniques adaptable for high-yield production of next-generation ion-traps.
- Process design kits (PDKs) for fabricating next-generation ion-traps using standardized building blocks. Integrating cutting-edge PDKs with European virtual design platforms to standardize production and reduce the need for custom developments.
- Integration of advanced features such as segments and junctions, and integrated photonics for addressing, manipulation, and readout in ion-trap chips.
- Enhancing technology (including enabling technologies) and manufacturing readiness levels across the quantum industry, addressing applications in one or more of the following: quantum computing, communications, simulation, and/or sensing.
- Standardization of production processes and development of high-quality ion-traps for diverse applications including quantum computing, quantum communication, quantum metrology, and quantum simulation.
- Demonstration of scalable, efficient, and stable (e.g. high yield) production capabilities. The development of robust and repeatable manufacturing processes tailored to quantum chips' unique requirements, enabling a consistent and reliable supply for European stakeholders.
- Developing reliable characterization tools to ensure quality assurance of trapped-ion chips, ensuring consistency and reliability across production batches, and demonstrating the scalability of pilot line technologies from small-to-mid volume fabrication to potentially large-scale industrial production.
- Define a technology roadmap and implementation plan towards industrialisation of the production of quantum chips.

Proposals should outline strategies for:

- Preparing production sites and procuring advanced manufacturing equipment.
- Extensive testing and quality assurance to align with European quantum initiatives.
- Integrating photonics or electronics into ion-traps, enhancing their functionality at ultrahigh-vacuum or cryogenic temperatures.
- Developing comprehensive production lifecycle processes from design to final assembly and testing, ensuring mass production capability.

3.6.5. Eligibility

In order to achieve the expected outcomes, and safeguard the Union’s strategic assets, interests, autonomy, and security, it is important to avoid a situation of technological dependency on a non-EU source, in a global context that requires the EU to take action to build on its strengths, and to carefully assess and address any strategic weaknesses, vulnerabilities and high-risk dependencies which put at risk the attainment of its ambitions.

For this reason, participation is limited to legal entities established in Member States, Iceland, Norway and the following additional associated country: Israel.[35]

For the duly justified and exceptional reasons listed in the previous paragraph, in order to guarantee the protection of the strategic interests of the Union and its Member States, entities established in an eligible country listed above, but which are directly or indirectly controlled by a non-eligible country or by a non-eligible country entity, may not participate in the action unless it can be demonstrated, by means of guarantees provided by their eligible country of establishment, that their participation to the action would not negatively impact the Union's strategic, assets, interests, autonomy, or security.[36]

3.6.6. STEP and sovereignty seal

This topic contributes to the objectives of the *Strategic Technologies for Europe Platform* (STEP). As such, eligible proposals that exceed the evaluation thresholds will be awarded a *Sovereignty Seal*. The Sovereignty Seal is a quality label, valid for the duration of the project, which will facilitate access to additional EU funding (alternative, cumulative or combined funding from several EU budget instruments) or national public and private investments.

3.6.7. Specific provisions applicable to this Call

The following points on access conditions apply.

35 Legal entities established in Israel are eligible to participate in this action on the basis that (i) Israel is an associated country (and continues to be on the date of the opening of this topic for submission); and (ii) Israel meets specific conditions. Prior to the adoption of this Work Programme, questionnaires were sent to non-EEA associated countries and countries in the process of association in order to assess their eligibility to participate.

36 The guarantees shall in particular substantiate that, for the purpose of the action, measures are in place to ensure that:

a) control over the applicant legal entity is not exercised in a manner that retrains or restricts its ability to carry out the action and to deliver results, that imposes restrictions concerning its infrastructure, facilities, assets, resources, intellectual property or know-how needed for the purpose of the action, or that undermines its capabilities and standards necessary to carry out the action;

b) access by a non-eligible country or by a non-eligible country entity to sensitive information relating to the action is prevented; and the employees or other persons involved in the action have a national security clearance issued by an eligible country, where appropriate;

c) ownership of the intellectual property arising from, and the results of, the action remain within the recipient during and after completion of the action, are not subject to control or restrictions by noneligible countries or non-eligible country entity, and are not exported outside the eligible countries, nor is access to them from outside the eligible countries granted, without the approval of the eligible country in which the legal entity is established.

3.6.7.1. Access conditions for pilot lines

Access to the pilot lines should be based on fair and non-discriminatory principles and should be limited to Participating States of the Chips JU, meaning EU MS, EEAs and those countries that have been associated to Horizon Europe, under which the pilot lines are funded. In determining access to the pilot lines for users established in any Participating State but controlled from third countries that are not Participating States of the Chips JU, the consortium must take into consideration the following two main criteria:

1. EU added value, i.e., their contribution to the objectives of the Chips Act as set out in Article 4.

2. Economic security considerations.

The above access criteria should also be duly considering other relevant provisions of the Chips Act Regulation (notably Recital 11[37], and Recital 27[38], such as for example those in relation to

37 It is a clear objective of the Union to promote international cooperation and knowledge exchange on the basis of the Union's interests, mutual benefits, international commitments, and, to the extent possible, reciprocity. Nevertheless, the infringement of intellectual property (IP) rights, the unauthorised disclosure of trade secrets, or the leakage of sensitive emerging technologies in the semiconductor sector could compromise the interests of the security of the Union. Against this background, the Commission is exploring concrete proposals to strengthen the Union's investment and export control frameworks. In addition, the Union and the Member States should cooperate with strategic partners to strengthen the joint technological and industrial leadership in accordance with applicable procedural requirements.

38 R&D within the Union is increasingly exposed to practices aiming to misappropriate confidential information, trade secrets, and protected data, such as IP theft, forced technology transfers and economic espionage. In order to prevent adverse impacts on the interests of the Union and the objectives of the Initiative, it is necessary to adopt an approach to ensure that the access to and use of sensitive information or results, including data and know-how, security and transfer of ownership of results as well as content protected by IP rights generated in connection to or as a result of actions supported by the Initiative, are protected. To ensure that protection, any actions supported by the Initiative and funded by Horizon Europe and the Digital Europe Programme should follow the relevant provisions of those Programmes, such as on participation of entities established in third countries associated with the programme, grant agreements, ownership and protection, security, exploitation and dissemination, transfer and licensing and access rights. It is possible to set specific provisions when implementing those Programmes, in particular with regard to limitations to transfers and licensing in accordance with Article 40(4) of Regulation (EU) 2021/695, and limitation of participation of legal entities established in specified associated or other third countries due to reasons based on the Union's and the Member States' strategic assets, interests, autonomy or security, in accordance with Article 22(5) of Regulation (EU) 2021/695 and Article 12(6) of Regulation (EU) 2021/694. Additionally, the handling of sensitive information, security, confidentiality, protection of trade secrets and IP rights should be governed by Union law, including Directives (EU) 2016/943 (11) and 2004/48/EC ( ) of the European Parliament and of the Council, and national law. It is possible for the Commission and the Member States to protect technology transfers for reasons related to Union and national security interests in relation to investments made in facilities falling within the scope of this Regulation in accordance with Regulation (EU) 2019/452 of the European Parliament and of the Council (12 13).

the handling of sensitive information, potential risks of infringement of intellectual property (IP) rights, unauthorised disclosure of trade secrets and IP rights, security, confidentiality, or the leakage of sensitive emerging technologies within the semiconductor sector.

Only users from organisations that can clearly demonstrate their contribution to EU added value, their alignment with European economic security shall be granted access. Users from third countries will be granted access when this is foreseen in the international obligations of the Union concerning semiconductors, as these defined in any relevant Digital Partnerships or Trade and Technology Council agreements. In this case, such users should still commit to fulfil the above access criteria.

In close collaboration with the Commission, the selected consortia will be tasked to further elaborate on the above access criteria as well as access conditions and widely publish them.

CALL FOR PILOT LINES (CPL)

Proposals for the pilot lines will be collected through a Call for Pilot Line (CPL).

The document describing the CPL and every facet of this call including the necessary elements for the 3 interrelated calls is included in this chapter and will be used to launch the calls as it contains the details of the procedure.

To launch the calls, the call for the Pilot Line on Advanced Photonic Integrated Circuits will merge the technical description of the topic and specific budgets given in chapter 2.4 with the Call Document in this chapter. The Annexes mentioned in this chapter are collected at the end of this document.

Call text

Chips Joint Undertaking

REF: Chips-2024-CPL-5

CALL FOR PILOT LINE ON ADVANCED PHOTONIC INTEGRATED CIRCUITS

3. INTRODUCTION – CONTEXT AND BACKGROUND

3.1. LEGAL FRAMEWORK

The Chips Joint Undertaking (hereinafter "Chips JU") is established by Council Regulation (EU) 2021/2085 establishing the Joint Undertakings under Horizon Europe[39] (hereinafter "SBA") and modified by an amendment, Council Regulation (EU) 2023/1782 of 25 July 2023[40].

The Chips for Europe Initiative is established under Regulation (EU) 2023/1781 of 13 September 2023[41] (hereinafter "Chips Act"). One objective of the Chips Act is to ensure the conditions necessary for the competitiveness and innovation capacity of the Union. In this context, the Chips for Europe Initiative (the 'Initiative') established by the Chips Act aims to support this objective by bridging the gap between the Union's advanced research and innovation capabilities and their sustainable industrial exploitation.

The Initiative shall promote capacity building to enable design, production and systems integration in next-generation semiconductor technologies, and should enhance collaboration among key players across the Union, strengthening the Union's semiconductor supply and value chains, serving key industrial sectors and creating new markets.

Pilot lines are one of the components of the Initiative. Concretely, the Initiative will support the enhancement of existing and development of new advanced pilot lines to enable development and deployment of cutting-edge semiconductor technologies and next-generation semiconductor technologies. These pilot lines shall provide for the industry a facility to test, experiment and validate semiconductor technologies and system design concepts.

39 OJ L 427, 30.11.2021, p. 17–119.

40 OJ L 229, 18.9.2023, p. 55–62.

41 OJ L 229, 18.9.2023, p. 1–53.

The above is further defined in Article 3 ("Establishment of the Initiative"), Article 4 ("Objectives of the Initiative") and Article 5 ("Content of the Initiative") of the Chips Act. Article 4(2)(b) makes reference to "operational objective 2" which mentions "*enhancing existing and developing new advanced pilot lines across the Union to enable development and deployment of cutting-edge semiconductor technologies and next-generation semiconductor technologies*". Article 5(b) further specifies the content of this operational objective on pilot lines, namely that "*the Initiative shall, under its operational objective 2*:

(i) *strengthen capabilities in next-generation chip production technologies and manufacturing equipment, by integrating research and innovation activities and preparing the development of future technology nodes, such as leading-edge nodes, fully depleted silicon on insulator technologies, new semiconductors materials or heterogeneous systems integration and advanced module assembly and packaging for high, medium or low volumes;*

(ii) *support innovation at a large scale through access to new or existing pilot lines for experimentation, test, process control, final device reliability and validation of new design concepts integrating key functionalities;*

(iii) *provide support to integrated production facilities and open EU foundries through preferential access to the new pilot lines, as well as ensure access on fair terms to new pilot lines for a wide range of users of the Union's semiconductor ecosystem".*

Article 12(1) of the Chips Act entrusts the implementation of the Initiative's operational objectives 1-4 to the Chips JU. Therefore, operational objective 2 on pilot lines will be implemented by the Chips JU.

3.1.1. Budget

The Chips JU proceeds to the implementation of pilot lines which will be co-financed by the Union and the participating states. The Chips JU shall be tasked with providing financial support, through any instrument or procedure provided for in Horizon Europe[42] (hereinafter "HE") and the Digital Europe Programme[43] (hereinafter "DEP").

In accordance with recital (6) of the SBA Amendment, throughout the lifetime of the Chips Joint Undertaking, up to EUR 2,875 billion shall be dedicated to the Initiative. Of that amount, EUR 1,450 billion shall be for capacity-building activities for operational objectives 1 to 4 and

42 Regulation (EU) 2021/695 of 28 April 2021 establishing Horizon Europe – the Framework Programme for Research and Innovation, laying down its rules for participation and dissemination, and repealing Regulations (EU) No 1290/2013 and (EU) No 1291/2013

43 Regulation (EU) 2021/694 of 29 April 2021 establishing the Digital Europe Programme and repealing Decision (EU) 2015/2240

EUR 1,425 billion shall be for research and innovation activities related to operational objectives 1 to 4.

Furthermore, Article 128(4) of the SBA Amendment indicates that the Union's contribution from DEP may not exceed 50% of the total costs of capacity-building activities.

It must be noted as well that, in accordance with Article 129(4) of the SBA Amendment, the participating states are allowed to report financial contributions made since 8 February 2022 (date of publication of the Chips Act package), and until the date of signature of the Hosting Agreement, if the conditions set out in Article 129(4) SBA are fulfilled. In their applications, applicants need to specify what costs would be within the scope of this Article.

3.1.2. The overall implementation process

Implementing an advanced pilot line is a complex endeavour requiring a coordinated effort of multiple procurements of equipment and tools, as well as set-up and integration activities related to those equipment and tools to achieve a specific technologically advanced infrastructure that then can be used by industry, both large enterprises, SMEs and startups, as well as academia.

Given the important role that a pilot line has in bridging the gap between the Union's advanced research and innovation capabilities and their sustainable industrial exploitation, the Chips Joint Undertaking should co-own 50% of the tools and equipment that constitute a pilot line as permitted by Article 3(4) of the SBA and Article 43(5) of the Financial Rules of the Chips JU [44]. This will allow the Chips Joint Undertaking to keep a closer control over such strategic infrastructures, thereby making future reporting exercises towards auditing authorities more transparent and straightforward.

3.1.2.1.The Hosting Consortium

A consortium needs to include:

a) at least one independent legal entity established in a Member State; and
b) at least two other independent legal entities each established in different Participating States[45].

Furthermore, the consortium (hereinafter 'Hosting Consortium'), will be composed of one or more Hosting Entities (i.e., entities that are hosting part or all of the equipment and tools of the pilot line – see further below) and possibly other members (members of the consortium that do not host any tools and equipment of the pilot line). One of the consortium members acts as the coordinator; typically, but not necessarily, the coordinator is a Hosting Entity. The coordinator

44 Chips GB decision 2021.02 (Annex 12) approving the Financial Rules, re-adopting the previously adopted decision ECSEL GB 2020.138 (see link)

45 It must be noted that entities established in Participating States that are associated countries (i.e., not in a Member State) will only receive funding from the Programme (HE and/or DEP) their countries are associated to.

will be mandated by the Hosting Consortium to act on behalf of the other members of the consortium (e.g., to sign the Hosting Agreement – see Annex 2).

The pilot line can be physically located at one or several hosting sites. A hosting site is the physical facility at which a Hosting Entity will host and operate a pilot line and which is established in a Participating State that is a Member State. It must be noted that a pilot line may be distributed across different hosting sites that are located in different Member States.

A consortium including Hosting Entity(ies) will be selected for setting up and running a pilot line. The consortium will have as **main responsibilities**:

- to manage joint procurements, if certain conditions are fulfilled (see under Section 3.1.2.3.1): this requires having the necessary expertise and the staff to execute joint procurements;
- to install, commission and host the procured equipment and tools on the hosting site(s). Therefore, all hosting sites need to have the proper infrastructure (so-called cleanrooms and other technical facilities) and the proper staff;
- to execute (for pilot lines that are located on different sites, in a coordinated way) the different activities that will lead to a technologically advanced pilot line and to offer all its services (such as access by third parties, etc.) ultimately realising the objectives of the pilot line.

3.1.2.2.The present Call Document

Taking into account the abovementioned responsibilities, the present Call Document includes three interrelated calls:

- A **Call for Expression of Interest** (hereinafter "CfEoI") for the selection of a Hosting Consortium. Provided certain conditions are fulfilled by the Hosting Entity(ies) of the Hosting Consortium (see Section 3.1.2.3.1 below), this CfEoI will entitle the selected Hosting Entity(ies) to manage the procurement of the tools and equipment of the pilot line to be acquired under a joint procurement agreement (JPA – enclosed as Annex 3).
- A **Call for proposals for the Set-up, integration and process development** grant funded under the Horizon Europe Programme. The type of action is a Research and Innovation Action (RIA).
- A **Call for proposals for the operational activities** of the pilot line, funded under the Digital Europe Programme. The type of action is a Simple Grant.

In practice, to cover the activities needed for a pilot line, consortia would submit three interrelated proposals, one for each of the abovementioned calls. Each call will have its specific admissibility requirements and eligibility, exclusion, and evaluation criteria, as outlined in this document. Consortia submitting proposals to calls for proposals may be different from Hosting Consortia submitting proposals for the Call for Expression of Interest as long as admissibility requirements and eligibility and exclusion criteria of the funding programmes concerned are respected.

All three calls will close on the same date.

Together with the present Call Document, the following documents[46] are published:

Annex 1	Application form template
Annex 2	Draft Model Hosting Agreement
Annex 3	Draft Model Joint Procurement Agreement
Annex 4	Model Letter of Intent describing the formal commitment of each Participating State (PS) to financially support the pilot line and its participating Consortium members
Annex 5	HE model grant agreement for the R&D activities of the pilot line
Annex 6	DEP model grant agreement for the operational activities of the pilot line

In addition to the above documents which are annexed to the present Call Document, additional documents will be published that are relevant in case of State aid notification. These documents should not be submitted to any of the three calls above. These documents are:

- Funding gap template;
- Notification template, which indicates the information a Member State needs to provide (see Section 3.1.2.3.5).

3.1.2.3.Submission of an application to the present Call Document

Applicants may submit applications to the present Call Document by filling in the ***application form (Annex 1 to the present Call Document)***. The application should serve as:

- An expression of interest to be submitted to the Call for Expression of Interest for the selection of a Hosting Consortium for the pilot line;
- A proposal to be submitted to the Call for Proposals for Set-up, integration and process development (Horizon Europe, Research and Innovation Action);
- A proposal to be submitted to the Call for Proposals for Operational activities of the pilot line (Digital Europe Programme, Simple Grant).

The expression of interest for the selection of a Hosting Consortium will be evaluated by a group of independent experts[47] in accordance with the evaluation criteria set out in Section 3.7.

The selected Hosting Consortium may be eligible to receive the following two types of funding as long as its proposals pass the necessary thresholds.

46 Some of these documents are drafts. After the opening of the Call, updated drafts may be published on the JU's website. The final content of these drafts may be agreed upon together with the relevant signatories.

47 The group of independent experts that will evaluate the expression of interest for the selection of a Hosting Consortium may be the same group that evaluates the proposals for the Horizon Europe and Digital Europe Programme calls.

3.1.2.3.1. Funds for Joint Procurements – only for Hosting Entities

Joint procurements are managed by **Joint Procurement Agreements (JPA).** The JPA is an agreement between the Chips JU and the contracting authority of a Member State in order to set the rules to procure, in accordance with Article 165(2) FR, the tools and equipment from third-party vendors, that will be hosted by the Hosting Entity of that Member State.

It must be noted that there will be one JPA per Hosting Entity. This means that in a consortium with only one Hosting Entity there will only be one JPA while in a consortium with three Hosting Entities there would be one JPA for each Hosting Entity.

Given that in each JPA "*the share pertaining to or managed by the contracting authority of a Member State in the total estimated value of the contract will be equal to or above 50 %*" (Article 165(2) FR), the procedural rules applicable to the contracting authority of that Member State may apply to the joint procurement, provided that those rules may be considered as equivalent to those of the Union.

In this context, Member States have **two possible options** regarding who will act as contracting authority and therefore sign the JPA:

- **Option 1**: the joint procurement is carried out by the Member State in accordance with national procurement rules. In this case, given that the Member State itself will act as contracting authority, the JPA will be signed between the Chips JU and the Member State.

- **Option 2**: the joint procurement is carried out by the Member State, who decides to delegate the procurement process to the Hosting Entity established in that Member State, that will procure in the name and on behalf of the Member State. However, this option is only possible *as long as* the Hosting Entity can be considered a "contracting authority" within the meaning of the Procurement Directive[48]. In this case, the JU signs the JPA with the Hosting Entity, acting as contracting authority. The other members of the Hosting Consortium which are not Hosting Entity(ies) (i.e., do not have a hosting site with tools and equipment) may not in any event be signatories to the JPA and may not be involved in the procurement process.

In the abovementioned Model Letter of Intent, the Member State will have to indicate what option it intends to use and thus which entity it proposes as signatory of the JPA. In both cases, 50% of the procured tools and pieces of equipment of the pilot line shall be owned by the Chips JU. Regarding the remaining 50%, the Member State may decide to transfer its share of ownership to the relevant Hosting Entity.

48 Directive 2014/24/EU of the European Parliament and of the Council of 26 February 2014 on public procurement and repealing Directive 2004/18/EC.

3.1.2.3.2. Grants under the Horizon Europe and Digital Europe Programmes

As mentioned in Section 3.1.2.2, the present Call Document includes two calls for proposals for grants:

- **Set-up, integration and process development Grant**: this grant would cover the costs of deploying the infrastructure at a sufficient maturity level and the R&D&I activities required for the development of the process technology. This includes inter alia the cost to define tender specifications (for procurements), to integrate procured tools and equipment with existing facilities, to modify equipment, test, verify and validate the integration of the pilot line, and to develop the PDK/ADK (including its interfacing / deployment in the Design Platform). This grant will be established as a Horizon Europe Grant Agreement and will be evaluated according to Horizon Europe rules (See Section 3.7).

- **A Grant for the operational activities**: this grant would cover part of the operational activities of the pilot line, i.e., part of the standard operating costs of the pilot line. This grant will be established as a Digital Europe Programme Grant Agreement and will be evaluated according to the Digital Europe Programme rules (See Section 3.7).

Applicants must justify that no double funding is requested. Funding can only be provided on the condition that the prohibition on double funding is respected.

The proposals submitted to each of these calls and included in the application will be evaluated separately, possibly by the same group of independent experts. The results of these evaluations will be ranked lists.

EU funding rates are up to 50% for grants under the Digital Europe Programme, and up to 100% for grants under Horizon Europe.

3.1.2.3.3. The Hosting Agreement

On the basis of the abovementioned ranked lists, the Public Authorities Board (PAB) of the Chips JU will:

- Select the Hosting Consortium that will implement the pilot line;
- Award the grant for ‘Set-up, integration and process development’;
- Award the grant for the ‘Operational activities’.

Subsequently, the coordinator and the Chips JU will sign a ***Hosting Agreement.*** The Hosting Agreement is the contract that lays down the rules that shall apply to the Hosting Consortium in the context of the implementation of the pilot line. The Hosting Agreement and the conditions described therein are valid until the end of 2031 and may be renewed subject to additional funding under the next MFF.

However, before the signature of the Hosting Agreement (but after the selection of the Hosting Consortium by the PAB), the Chips JU and the Hosting Consortium may address and finetune

certain elements of the application. The final version agreed upon by the Chips JU and the Hosting Consortium will be the "Description of Action" which will be annexed to the Hosting Agreement and to the two Grant Agreements.

3.1.2.3.4. Responsibility and liability of the consortium

It must be noted that all members of a Hosting Consortium are jointly responsible for implementing the pilot line in line with the Hosting Agreement. To implement the action properly, they must make appropriate internal arrangements.

3.1.2.3.5. State aid

The fulfilment of State aid rules is a responsibility that pertains solely to the Member States. It is therefore their responsibility to assess whether the aid they intend to provide to the pilot line can be considered State aid and therefore potentially require a notification to the European Commission. Each case may be different and present similar but also slightly different characteristics.

3.2. OBJECTIVES

The overall objective of the present Call Document is to select a Hosting Consortium in order to implement the pilot line in line with Section 3.1.2.

The Pilot Line "Title of the pilot line" to be implemented is described below.

A key element of the pilot line is to serve as a bridge from the lab to the fab, by providing industry a facility to test, experiment and validate semiconductor technologies and system design concepts. Such testing and experimentation would allow industry actors to test technologies for the development of new or improved products and processes. While the pilot lines is not expected to offer fully matured fabrication services, its evolution is crucial in aiding industry to refine and advance its processing techniques and prototype next generation devices.

Furthermore, the pilot line must provide the facility for industry to characterise and evaluate advanced processes and potential outputs stemming from their process technology in collaboration with the Hosting Consortium and in line with the conditions, including those related to access, set out in this Call Document. The Hosting Consortium is required to specify the terms and conditions for any of the foreseen collaborations with industry.

To this end, Hosting Consortia are invited to submit proposals for the three calls that take into consideration collaboration with industry and other relevant stakeholders established in the Union – and where justified beyond – by credibly addressing several or all of the following elements:

- **Process development**: describe planned collaboration with equipment manufacturers in the development of next-generation equipment related to the process technology being developed on the pilot line.
- **Process technology**: provide a roadmap for the eventual transfer of elements or all of the process technology to industrial partners in their deployment of mass-production facilities.
- **Development**: list potential development, including collaborative development involving the Hosting Consortium, of prototype devices on the pilot line infrastructure. Additionally, include a detailed description of the assistance the Hosting Consortium offers to users of the pilot line.
- **Skills development**: give an overview of the plans for developing technical skills and operational know-how, particularly in relation to process development, process technology, and designing, creating, and refining semiconductor devices, and the anticipated spill-over effect of strengthening the European workforce to the benefit of European industry.
- **Research output**: provide an overview of all the expected research collaborations with industry, other RTOs, and academic institutions, and the foreseen outputs.

3.2.1. Description of the pilot line

The description of the pilot line is given in Section 2.3 in the Work Programme part above.

3.2.2. Budget available

The Union financial contribution to the Chips JU for the implementation of the Pilot Line shall cover up to 50 % of the total costs of the pilot line. The remaining total cost of the pilot line (including VAT if applicable) shall be covered by the members of the Hosting Consortium and/or by the Participating State(s) where the Hosting Consortium members are established.

The total maximum EU budget is as follows:

- Joint procurements of equipment and tools: up to EUR XXX million from the Digital Europe Programme;
- Set-up, integration and process development: up to EUR XXX million from Horizon Europe;
- Operational activities: up to EUR XXX million from the Digital Europe Programme.
- Total pilot line: up to EUR XXX million.

The respective amounts for the pilot lines are given in Section 2.3 in the Work Programme part above.

The sum of the EU budgets requested in the proposals for the three parts above (joint procurement, Horizon Europe grant, Digital Europe Programme grant) in an application may not exceed the total maximum EU budget above.

The Executive Director may adapt the amounts for the actions set out in Section 3.3 based on the amounts requested in the submissions received.

3.3. CONTENTS OF THE APPLICATION

An application must be submitted using the application form included as Annex 1 to this call. As indicated above, the application should include:

- An expression of interest for the Call for Expression of Interest for the selection of a Hosting Consortium for the pilot line;
- A proposal for the Call for Proposals (CfP) for Set-up, integration and process development (Horizon Europe);
- A proposal for the Call for Proposals (CfP) for Operational activities of the pilot line (Digital Europe Programme).

The application needs to contain the following information, amongst other potential considerations:

- **Detailed description and timeline**: An overview of the pilot line infrastructure, with details on the phased implementation approach of the project in terms of a *technology roadmap*. Furthermore, the proposal shall include a description of the major phases of the pilot line's development highlighting equipment acquisition, procurement timing, process development, integration, testing, validation, operationalisation and the possible development of demonstrators within the context of a work plan. Such a roadmap and work plan shall mainly include two phases:
  - a **development phase**, i.e., the procurement, set-up, engineering and integration efforts and process development required for preparing the pilot line to become fully operational (mostly relevant for the CfP for Set-up, integration and process development); and,
  - an **operational phase**, i.e., the efforts related to the access and service provisioning of the pilot line to the wider community of the pilot line (mostly relevant for the CfP for Operational activities).

- **Collaboration**: Each pilot line shall make an effort to have spill-overs beyond its immediate scope and involve a number of relevant stakeholders from across the Union (mostly relevant for the CfP for Set-up, integration and process development).
  - Collaboration with other pilot lines: by ensuring complementarity and, where possible, identify methods of amalgamation of activities.
  - Collaboration with RTOs and academia: by ensuring research partnerships with relevant research organisations thereby ensuring spill-over effects. Pilot lines should also strive to work with universities and training institutions in skills development.

- **Management of the distributed elements** of the pilot line (if any): The proposal needs to

clearly explain the terms of collaboration between the different members of the consortium and shall provide a credible description of how distributed elements of the pilot line will work in synergy together as one pilot line in an efficient manner that enables European added value (mostly relevant for the CfP for Set-up, integration and process development).

- **Business model**: A description of the business model related to the functioning (i.e., service provisioning) of the pilot line, once it has been set up. The business model must outline a reasonable breakdown of the expected income via market-oriented access conditions. It should clarify how these revenues will contribute to covering a portion or the entirety of the operational expenses associated with the pilot line (mostly relevant for the CfP for Operational activities).

- **Access conditions**: Detailed description of the access conditions to be applied by the pilot line, based on the boundary conditions set by the legal acts, the work programme, and the international obligations of the EU (mostly relevant for the CfP for Operational activities). Furthermore, following Article 128(5) SBA Amendment, applicants are reminded of the following guiding principles:
  - Inclusivity: access to the facilities, resources, and expertise related to the pilot line should be available to a diverse range of users across the European Union. This inclusivity extends to stakeholders from academia, industry, research institutions, and any other entities that are interested in the pilot line.
  - Transparency: Information regarding the criteria, processes, and terms governing access to the pilot line shall be clear and transparent to ensure that potential users have a comprehensive understanding of the access framework.
  - Non-Discrimination: Access shall be granted on a non-discriminatory basis, avoiding preferential treatment of potential users based on their geographic location, affiliation, etc.

Furthermore, the following provisions need to be catered for:

- To further advance the principles outlined above, access to the pilot line by users established in the Union shall be directly proportional to the financial contribution made by the European Union to cover the costs of the proposed project.
- Recognising the role played by Small and Medium-sized Enterprises (SMEs) in driving innovation and economic growth, a Hosting Consortium needs to grant preferential access or reduced prices to SMEs, including startups, as well as to academic institutions. Applicants may establish a differentiated pricing structure specifically tailored to accommodate the financial capacity of SMEs and academic institutes. This approach would facilitate the engagement of SMEs and academic institutions by ensuring that cost barriers do not impede their ability to access the pilot line. Access to the pilot line at preferential conditions for SMEs and academic institutions should be guaranteed until the duration of the Hosting Agreement, possibly after the end of funded activities.

  - In determining access to the pilot line for users established in any Participating State but controlled from third countries that are not Participating States of the Chips JU, the consortium must take into consideration EU added value, i.e. their contribution to the objectives of the Chips Act as set out in Article 4, and economic security considerations.
  - Applicants need to anticipate potential situations of excessive demand for access to the pilot line, putting in place mechanisms to ensure fairness, transparency, and equal opportunity for all interested parties. The proposal needs to establish clear procedures for managing and mitigating excessive demand, which may include collaboration with external partners, expansion of capacity where feasible, etc.
  - In accordance with Article 5(b)(iii) Chips Act, the Hosting Consortium needs to provide support to integrated production facilities and open EU foundries through preferential access to the pilot line, as well as ensure access on fair terms for a wide range of users of the Union's semiconductor ecosystem.
  - Access should be foreseen for international research and commercial partners (in line with Recital (18) Chips Act), in particular taking into account Union policies that affect the European semiconductor ecosystem, such as certain Digital Partnerships and Trade and Technology Councils.
  - Access to the pilot line shall also be granted in relation to virtual assets, including but not limited to Process Design Kits (PDKs), Assembly Design Kits (ADKs), and their corresponding documentation, emanating from its development. Applicants need to elaborate on the methods by which such access will be realised and present the degree of openness of the access policy governing the diverse components of the PDK/ADK.

- **Procurement of equipment (CAPEX)**: The (rough) costings and technical specifications of each tool and piece of equipment that shall be procured from third-party vendors. It should also be indicated what costs fall within the scope of Article 129(4) of the SBA Amendment on retroactivity (mostly relevant to the Call for Expression of Interest).

- **Set-up, integration and process development (RDI activities)**: A description of the work required for the set-up, integration, and process development, as well as for the testing and validation of the process technology activities including costs until the pilot line is at a sufficient level of maturity such that it can be considered operational. Set-up and integration costs should be related to the corresponding piece of equipment (where relevant). This includes an overview of how the pilot line will be interfaced with the broader community through PDKs/ADKs, technology interfaces etc. The hosting consortium needs to ensure the availability of the PDKs/ADKs in the Design Platform and sufficient integration with relevant EDA tools.

- **Operational activities**: A description of the activities related to the operational phase of the pilot line (i.e., the service provisioning of the pilot line to the wider community), the expected engagement with third parties and an estimate of the costs and possible funding

required for the satisfactory operation and use of the common infrastructure. Here, costs may include the expenses related to the operation of the heavy equipment and cleanrooms, i.e., maintenance, energy/electricity, personnel costs for running the pilot line. The proposal needs to contain a business model that considers expected future revenues based on appropriately defined access conditions, explaining how such revenues will cover part or all of the pilot line's operational expenses.

- **Budget**: A detailed line-by-line breakdown of all costs that shall be categorised in three categories: (i) CAPEX; (ii) set-up, integration and process development costs; and (iii) operational costs. The proposal must include a distribution of the budget for the three categories over time, with a planning horizon of at least 5 years.

- **Exploitation plans**: Detailed exploitation plans for the pilot line beyond the period of financial support from the Chips JU (including potential support financed under the next MFF). These plans need to include:
  - A description clearly indicating the sustainability of the pilot line beyond what will be financed in the current MFF.
  - Prospective plans and costs for modification/extension of the pilot line's infrastructure beyond the current MFF, where applicable.
  - Prospective estimates for the costs for its operation / usage by third parties beyond the current MFF.

- **Synergies with the Chips Act**: Clarification of the links to the broader Chips for Europe Initiative activities, such as the Design Platform, Competence Centres, and skills development.

In addition to the above, any application submitted by the hosting consortium should be accompanied by **Letters of Intent** from the relevant public authorities of all Participating States supporting the Hosting Consortium and its application for a pilot line.

Such letters should specify the Participating States' financial commitments for the necessary national co-funding for the acquisition, set-up and integration, and operation of the pilot line. The letters should also define whether, in line with Article 165(2) Financial Regulation, the Member State in which a Hosting Entity is established[49] carries out the joint-procurement procedure itself (as contracting authority) or whether it delegates the procedure to the Hosting Entity. The latter case is only possible as long as the Hosting Entity can be considered a contracting authority within the meaning of the Procurement Directive. **The Letters of Intent must also specify clearly that the Member State supports that the Chips JU co-owns 50% of the tools and equipment of the pilot line.**

49 Hosting Entities must be established in Participating States that are Member States.

3.4. ADMISSIBILITY REQUIREMENTS

An application for the call for pilot line is not admissible if it has not been introduced under the 3 calls.

There are no page limits for the application but the consortia are encouraged to limit the narrative part of the application to 200 pages excluding the tables that are expected.

3.4.1. Admissibility requirements for the Call for Expression of Interest

To be admissible:

a) An application must be submitted no later than the **17 September 2024 at 17:00:00 Brussels time.**
b) An application must be submitted electronically (see section "Procedure for the submission"), using the application form in the Annex 1 (Chips JU Application Form)
c) An application must be submitted as described in Section 3.10;
d) The application is written in English.

Failure to comply with those admissibility requirements will lead to the rejection of the application.

Furthermore, the submitted application needs to be accompanied by the requested Letters of Intent from the Participating States supporting the Hosting Consortium.

3.4.2. Admissibility requirements for the Call for Proposals for Set-up, integration and process development

Admissibility conditions for this call follow the standard Horizon Europe admissibility conditions as stated in Annex A and Annex E of the Horizon Europe Work Programme General Annexes[50], with the exception of any page limits. Submission needs to follow the provisions in Section 3.10.

3.4.3. Admissibility requirements for the Call for Proposals for Operational activities of the pilot line

Proposals must be submitted before the call deadline **17 September 2024 at 17:00:00 Brussels time.**

Proposals must be complete and contain all the requested information and all required annexes and supporting documents and follow the Application Form.

50 https://ec.europa.eu/info/funding-tenders/opportunities/docs/2021-2027/horizon/wp-call/2023-2024/wp-13-general-annexes_horizon-2023-2024_en.pdf

At proposal submission, the coordinator will have to confirm that it has the mandate to act for all applicants. Moreover, the coordinator will have to confirm that the information in the application is correct and complete and that the participants comply with the conditions for receiving EU funding (especially eligibility, financial and operational capacity, exclusion, etc). Before signing the grant, each beneficiary and affiliated entity will have to confirm this again by signing a declaration of honour (DoH). Proposals without full support will be rejected.

The application must be readable, accessible and printable.

Applicants may be asked at a later stage for further documents (for legal entity validation, financial capacity check, bank account validation, etc).

3.5. ELIGIBILITY CRITERIA

3.5.1. Eligibility criteria for the Call for Expression of Interest

The call is open to entities or consortia of entities fulfilling cumulatively the following conditions:

a) The Hosting Consortium shall include the members that will host and operate the pilot line. The members of the consortium shall be from a Participating State to the Chips JU.
b) A consortium must consist of:
(a) at least one independent legal entity established in a Member State; and
(b) at least two other independent legal entities each established in a different Participating State;
c) The members of the Hosting Consortium shall be registered as a legal entity in one of the Participating States;
d) The applicant(s) shall have a legal personality on the date of the deadline for submission of applications and must be able to demonstrate their existence as a legal person.
e) Applications shall include the provision of appropriate supporting documentation proving for each member of the Hosting Consortium that the commitment of the Participating State(s) where the member(s) of the consortium is/are established will cover the share of the total cost of implementation of the pilot line that is not covered by the Union contribution referred to in Article 128 of the SBA.

In its application, the coordinator must be given a mandate to represent the other members of the Hosting Consortium to sign and administrate the Hosting Agreement and the various associated grants.

To assess the applicants' eligibility, the following supporting documents are requested:

- The legal entity identification form[51] duly completed and signed by the person authorized

51 http://ec.europa.eu/budget/contracts_grants/info_contracts/legal_entities/legal_entities_en.cfm

to enter into legally binding commitments on behalf of the applicant organization(s) to be submitted in original or a PIC number;

The following entities will be considered as non-eligible:

- natural persons;
- entities without legal personality.

3.5.2. Eligibility criteria for the Call for Proposals for Set-up, integration and process development

Eligibility criteria for this call follow the standard Horizon Europe eligibility criteria as stated in Annex B of the Horizon Europe Work Programme General Annexes[52].

3.5.3. Eligibility criteria for the Call for Proposals for Operational activities of the pilot line

Eligible participants (eligible countries)

In order to be eligible, the applicants (beneficiaries and affiliated entities) must:

- be legal entities (public or private bodies)
- be established in one of the eligible countries, i.e.:
    - EU Member States (including overseas countries and territories (OCTs))
    - non- EU countries:
        - EEA countries (Norway, Iceland, Liechtenstein)
        - countries associated to the Digital Europe Programme Specific Objective 6 or countries which are in ongoing negotiations for an association agreement and where the agreement enters into force before grant signature.

Beneficiaries and affiliated entities must register in the Participant Register — before submitting the proposal — and will have to be validated by the Central Validation Service (REA Validation). For the validation, they will be requested to upload documents showing legal status and origin.

Moreover, participation in any capacity (as beneficiary, affiliated entity, associated partner, subcontractor or recipient of financial support to third parties) is limited to entities established in eligible countries.

52 https://ec.europa.eu/info/funding-tenders/opportunities/docs/2021-2027/horizon/wp-call/2023-2024/wp-13-general-annexes_horizon-2023-2024_en.pdf

3.6. EXCLUSION CRITERIA

3.6.1. Exclusion criteria for the Call for Expression of Interest

There are no specific exclusion criteria for the Call for Expression of Interest.

3.6.2. Exclusion and selection criteria for the Call for Proposals for Set-up, integration and process development

Criteria related to financial and operational capacity and exclusion are described in Annex C of the Horizon Europe Work Programme General Annexes[53].

3.6.3. Selection and exclusion criteria for the Call for Proposals for Operational activities of the pilot line

Financial capacity

Applicants must have stable and sufficient resources to successfully implement the projects and contribute their share. Organisations participating in several projects must have sufficient capacity to implement all these projects.

The financial capacity check will be carried out on the basis of the documents applicants will be requested to upload in the Participant Register during grant preparation (e.g. profit and loss account and balance sheet, business plan, audit report produced by an approved external auditor, certifying the accounts for the last closed financial year, etc). The analysis will be based on neutral financial indicators, but will also take into account other aspects, such as dependency on EU funding and deficit and revenue in previous years.

The check will normally be done for all beneficiaries, except:

- public bodies (entities established as public body under national law, including local, regional or national authorities) or international organisations.
- if the individual requested grant amount is not more than EUR 60 000.

If needed, it may also be done for affiliated entities.

If the JU considers that your financial capacity is not satisfactory, it may require:

- further information
- prefinancing paid in instalments.
- (one or more) prefinancing guarantees.

or

- propose no prefinancing
- request that you are replaced or, if needed, reject the entire proposal.

53 https://ec.europa.eu/info/funding-tenders/opportunities/docs/2021-2027/horizon/wp-call/2023-2024/wp-13-general-annexes_horizon-2023-2024_en.pdf

Operational capacity

Applicants must have the know-how, qualifications and resources to successfully implement the project and contribute their share (including sufficient experience in projects of comparable size and nature).

This capacity will be assessed together with the 'Implementation' award criterion, on the basis of the competence and experience of the applicants and their project teams, including operational resources (human, technical and other) or, exceptionally, the measures proposed to obtain it by the time the task implementation starts.

If the evaluation of the award criterion is positive, the applicants are considered to have sufficient operational capacity.

Applicants will have to show their capacity via the following information:

- general profiles (qualifications and experiences) of the staff responsible for managing and implementing the project
- description of the consortium participants
- list of previous projects (key projects for the last 4 years).

Additional supporting documents may be requested, if needed to confirm the operational capacity of any applicant.

Exclusion

Applicants which are subject to an EU exclusion decision or in one of the following exclusion situations that bar them from receiving EU funding can NOT participate[54]:

- bankruptcy, winding up, affairs administered by the courts, arrangement with creditors, suspended business activities or other similar procedures (including procedures for persons with unlimited liability for the applicant's debts)
- in breach of social security or tax obligations (including if done by persons with unlimited liability for the applicant's debts)
- guilty of grave professional misconduct (including if done by persons having powers of representation, decision-making or control, beneficial owners or persons who are essential for the award/implementation of the grant
- committed fraud, corruption, links to a criminal organisation, money laundering, terrorism-related crimes (including terrorism financing), child labour or human trafficking (including if done by persons having powers of representation, decision-making or control, beneficial owners or persons who are essential for the award/implementation of the grant
- shown significant deficiencies in complying with main obligations under an EU procurement contract, grant agreement, prize, expert contract, or similar (including if done by persons having powers of representation, decision-making or control, beneficial owners

54 See Articles 136 and 141 of EU Financial Regulation

or persons who are essential for the award/implementation of the grant

- guilty of irregularities within the meaning of Article 1(2) of EU Regulation 2988/95 (including if done by persons having powers of representation, decision-making or control, beneficial owners or persons who are essential for the award/implementation of the grant)
- created under a different jurisdiction with the intent to circumvent fiscal, social or other legal obligations in the country of origin or created another entity with this purpose (including if done by persons having powers of representation, decision-making or control, beneficial owners or persons who are essential for the award/implementation of the grant).

Applicants will also be rejected if it turns out that[55]:

- during the award procedure they misrepresented information required as a condition for participating or failed to supply that information
- they were previously involved in the preparation of the call and this entails a distortion of competition that cannot be remedied otherwise (conflict of interest).

3.6.4. Rejection from the Call

The Executive Director of the Chips JU shall not conclude a Hosting Agreement with a consortium where:

- Any applicant has misrepresented the information required as a condition for participating in the procedure or has failed to supply that information.

The same exclusion criterion applies to affiliated entities.

Administrative sanctions (exclusion) may be imposed on applicants, or affiliated entities where applicable, if any of the declarations or information provided as a condition for participating in this procedure prove to be false.

3.7. EVALUATION CRITERIA

3.7.1. Evaluation criteria for the Call for Expression of Interest

This Section explains the evaluation criteria for the CfEoI. Eligible applications will be evaluated according to the following evaluation criteria:

1. **Excellence and relevance**
    - *Clarity and pertinence of the pilot line's objectives, and the extent to which the proposed pilot line complies with the general specifications, is ambitious, and goes beyond the state-of-the-art while being relevant for the Initiative and the other components of the Chips Act.*
    - *Soundness of the proposed methodology, including the underlying concepts, models, assumptions.*

55 See Article 141 EU Financial Regulation

- *Clarity and pertinence of the cooperation between the pilot line and the other actions under the Chips for Europe Initiative.*
- *Clarity and pertinence of access conditions and their practical implementation, including the business plan for covering the operational expenses related to access to the pilot line.*

2. **Impact**

The extent to which the outputs of the project shall contribute at the European and/or international level to:

- *Credibility of the pathways to achieve the expected outcomes and impacts, and the likely scale and significance of the contributions.*
- *Suitability and quality of the measures to maximize expected outcomes and impacts, as set out in the dissemination and exploitation plan, including communication activities.*
- *Credibility of the business model justifying the sustainability of operating the pilot line beyond the end of the project.*
- *Significant spill-overs that support the broader European semiconductor ecosystem.*

3. **Quality and efficiency of the implementation**

The following aspects will be considered:

- *Quality and effectiveness of the work plan, assessment of risks, and appropriateness of the effort assigned to work packages, and the resources overall.*
- *Capacity and role of each participant, and the extent to which the consortium brings together the necessary expertise.*

Experience of the Hosting Entity(ies) in implementing and operating similar systems;

- *Quality and pertinence of experience of the Hosting Entity in installing and operating similar systems.*
- *Extent that provided experience is sufficient for supporting the system described in the general system specifications.*

Quality of the hosting facility's physical infrastructure and;

- *Quality and pertinence of the current and proposed hosting facility's physical capacity and preparedness.*

Quality of service to the users, namely capability to comply with the service level agreement provided among the documents accompanying the selection procedure;

- *Quality and pertinence of service to the users, namely capability to comply with the service level agreement provided in the Hosting application.*
- *Quality of the proposed coordination and/or support measures to ensure requested service level towards pilot line users.*

Total cost of ownership of the pilot line and methodology to calculate it including an accurate estimate and a verification method of the set up and integration costs as well as the operating cost of the pilot line during its lifetime;

- *Clarity and effectiveness of the estimated cost of implementation of the application.*

- *Appropriateness of the methodology to calculate, report, validate and verify the operating costs.*

Criterion	Maximum score	Threshold
Excellence and Relevance	30	15
Impact	30	15
Quality and efficiency of the implementation including the Total Cost of Ownership	40	20
	100	60

Points will be allocated out of a total of 100 based on the table. Applications below these thresholds will be rejected.

3.7.2. Evaluation criteria for the Call for Proposals for Set-up, integration and process development

Award criteria for Research and Innovation Actions:

1. Excellence

- Clarity and pertinence of the project's objectives, and the extent to which the proposed work is ambitious and goes beyond the state of the art.
- Soundness of the proposed methodology, including the underlying concepts, models, assumptions, inter-disciplinary approaches, appropriate consideration of the gender dimension in research and innovation content, and the quality of open science practices, including sharing and management of research outputs and engagement of citizens, civil society and end-users where appropriate.

2. Impact

- Credibility of the pathways to achieve the expected outcomes and impacts specified in the work programme, and the likely scale and significance of the contributions from the project.
- Suitability and quality of the measures to maximise expected outcomes and impacts, as set out in the dissemination and exploitation plan, including communication activities.

3. Quality and efficiency of the implementation

- Quality and effectiveness of the work plan, assessment of risks, and appropriateness of the effort assigned to work packages, and the resources overall.
- Capacity and role of each participant, and the extent to which the consortium as a whole

brings together the necessary expertise.

Scores and weighting

Evaluation scores will be awarded for the criteria. For full applications, each criterion will be scored out of 5. The threshold for individual criteria will be 3. The overall threshold, applying to the sum of the three individual scores, will be 10. There is no weighting.

Proposals that pass the individual threshold AND the overall threshold will be considered for funding, within the limits of the available call budget. Other proposals will be rejected.

3.7.3. Evaluation criteria for the Call for Proposals for Operational activities of the pilot line

The award criteria for this call are as follows:

1. Relevance
- Alignment with the objectives and activities as described in section 3.2
- Contribution to long-term policy objectives, relevant policies and strategies, and synergies with activities at European and national level

2. Implementation
- Maturity of the project
- Soundness of the implementation plan and efficient use of resources
- Capacity of the applicants, and when applicable the consortium as a whole, to carry out the proposed work

3. Impact
- Extent to which the project will achieve the expected outcomes and deliverables referred to in the call for proposals and, where relevant, the plans to disseminate and communicate project achievements
- Extent to which the project will strengthen competitiveness and bring important benefits for society

Evaluation scores will be awarded for the criteria. For full applications, each criterion will be scored out of 5. The threshold for individual criteria will be 3. The overall threshold, applying to the sum of the three individual scores, will be 10. There is no weighting.

Proposals that pass the individual thresholds AND the overall threshold will be considered for funding within the limits of the available budget (i.e. up to the budget ceiling). Other proposals will be rejected.

3.8. OVERVIEW OF THE EVALUATION AND SELECTION PROCEDURE

The Chips JU is responsible for the implementation of the evaluations of the received applications. It organises the submission and evaluation procedures and communicates with the applicants.

The following describes this process. It is the same procedure for the Call for Expression of Interest, for the Call for Proposals for Set-up, integration and process development, as well as for the Call for Proposals for Operational activities of the pilot line.

3.8.1. Evaluation procedure

The submitted applications will be evaluated in a procedure by a panel of seven independent experts. These experts will be appointed by the Chips JU on the basis of the procedure followed under Digital Europe Programme and Horizon Europe (GB 2024.71). This generic procedure to appoint experts will be as well used for the Call for Expression of Interest. For the applications considered admissible according to Section 3.4, the Chips JU will assess the eligibility and exclusion criteria according to Sections 3.5 and 3.6 above. Only admissible and eligible applications will be evaluated.

- **Individual evaluations**: In the first step, the independent experts that sit on the panel shall carry out individually the evaluation of the applications based on the evaluation criteria described in Section 3.7 above. They give a score for each criterion, with explanatory comments. These individual reports form the basis of the further evaluation.
- **Consensus meetings**: After carrying out their individual assessment, all the experts that evaluated the applications shall convene in a consensus meeting, to agree on a common position, including comments and scores and prepare a consensus report. The consensus meetings shall be moderated by a Senior Programme Officer of the Chips JU who shall seek consensus, impartially, and ensure that all applications are evaluated fairly, in line with the relevant evaluation criteria.
- **Panel review**: The review panel shall be chaired by the Executive Director of the Chips JU. The panel will review the scores and comments for all applications to check for consistency across the evaluations. If necessary, it will propose a new set of marks or revise comments, and resolve cases where evaluators were unable to agree. The panel will prepare a final evaluation summary report.

3.8.2. Selection

The Executive Director of the Chips JU will review the results of the evaluation panels and will elaborate final ranking lists for each evaluation, based on the lists proposed by the panels.

This final ranking list shall consist of:

– a main list with the applications to be selected by the experts;

– a reserve list, with applications that have passed the evaluation thresholds.

In addition, the Chips JU will prepare a list with applications that did not pass the evaluation thresholds or were found to be ineligible.

The Executive Director will submit the final ranking lists, together with the Evaluation Summary Reports, to the Public Authorities Board of the Chips JU with a proposal for selection of the application, for approval by the Public Authorities Board.

The Public Authorities Board will make the final selection of consortia whose proposals were selected from submissions to the Call for Expression of Interest for the selection of a Hosting Consortium, the Call for proposals for the Set-up, integration and process development grant funded under the Horizon Europe Programme, and the Call for proposals for the operational activities of the pilot line, funded under the Digital Europe Programme.

After the decision of the Public Authorities Board, all applicants will be informed in writing by the Chips JU of the outcome of the evaluation in the form of Evaluation Summary Reports (ESR). The Chips JU will also inform about the final selection or rejection of applications.

The Chips JU will invite the coordinator of the selected Hosting Consortium to sign a Hosting Agreement with the Chips JU and to initiate grant agreement preparations. Grant agreements will only be concluded subject to the signature of the Hosting Agreement.

3.8.3. Communication

The information contained in the present call document provides all the information required to submit an application. Please read it carefully before doing so, paying particular attention to the priorities and objectives of the present call.

All enquiries must be made by e-mail only to: calls@chips-ju.europa.eu

Questions shall be sent to the above address no later than the **10 September 2024 17:00 Brussels time**, defined as "Deadline to submit questions about the Call" in Section 10.

The Chips JU has no obligation to provide clarifications to questions received after this date.

Replies will be given/published no later than the "Publication of the last answers to questions" defined in the timeline in Section 3.9.

To ensure equal treatment of applicants, the Chips JU will not give a prior opinion on the eligibility of applicants, or affiliated entity(ies), an action or specific activities.

No individual replies to questions will be sent but all questions together with the answers and other important notices will be published (FAQ in EN) at regular intervals on the website under the relevant call: https://www.chips-ju.europa.eu/Pilot-lines/

The Chips JU may, on its own initiative, inform interested parties of any error, inaccuracy, omission or clerical error in the text of the Call Document on the mentioned website. It is

therefore advisable to consult this website regularly in order to be informed of any updates and of the questions and answers published.

No modification to the applications is allowed once the deadline for submission has elapsed. If there is a need to clarify certain aspects or to correct clerical mistakes, the Chips JU may contact the applicant for this purpose during the evaluation process. This is generally done by e-mail. It is entirely the responsibility of applicants to ensure that all contact information provided is accurate and functioning.

In case of any change of contact details, please send an email with the application reference and the new contact details to calls@chips-ju.europa.eu.

In the case of hosting consortia, all communication regarding an application will be done with the coordinator only, unless there are specific reasons to do otherwise, where the consortium coordinator shall be in copy.

Applicants will be informed in writing about the results of the selection process. Unsuccessful applicants will be informed of the reasons for rejection. No information regarding the award procedure will be disclosed until the notification letters have been sent to the relevant applicants.

3.9. TIMETABLE

The steps and indicative times for the procedure from publication to expected start of the mandate for the selected Hosting Consortium are in the table below:

Selection of Hosting Consortium milestones	**Date and time or indicative period**
Call Document Publication	
Publication of this Call Document	25-07-2024
Submission of applications	
Calls Deadline	17-09-2024 - 17:00
Application Opening day (open of envelopes with expressions of interest)	
Evaluation	October 2024
Selection by Public Authorities Board	November 2024
Notification of results to applicants	
Signature of the hosting agreement	December 2024
Signature of hosting agreement	May 2025
Signature of grant agreements	

This schedule is common to the three interrelated calls: publication, submission, evaluation and selection dates are the same.

The timetable for the conclusion of the grant agreements is the same for the HE and DEP calls:

Information on the outcome of the evaluation	Maximum 5 months from the final date for submission
Indicative date for the signing of grant agreements	Maximum 8 months from the final date for submission

3.10. PROCEDURE FOR THE SUBMISSION OF APPLICATIONS

3.10.1. For the Call for Expression of Interest

Applications must be submitted no later than the 17 September 2024 at 17:00 Brussels time. Application forms are available at *[insert website]*.

Applications must be submitted in the correct form, duly completed and dated. They must be submitted in electronic copy on *[insert website]*. and signed by the person authorised to enter into legally binding commitments on behalf of the applicant organisation. The electronic version must contain the pdf versions of the application presented in paper and other files such as list of equipment (EXCEL spreadsheet), List of costs (EXCEL spreadsheet), etc.

Contact point for any questions[56] is calls@chips-ju.europa.eu.

3.10.2. For the Call HE

Applications submitted to EU funding & tender portal.

3.10.3. For the Call DEP

Applications submitted to EU funding & tender portal.

3.10.4. Other submission related comments

All applications will be treated confidentially, as well as any submitted related information, data, and documents. The Chips JU will ensure that the process of handling and evaluating applications is carried out in a confidential manner.

External experts are also bound by an obligation of confidentiality.

Applicants shall avoid taking any actions that could jeopardize confidentiality. They must not attempt to discuss their application with persons they believe may act as expert evaluator for the Chips JU.

Your application shall not contain any information that is 'EU classified' under the rules on security of information in the Commission security rules for protecting EU classified information (see also Classification of Information in DEP projects).

56 Questions on submission must be sent before the deadline indicated in Section 3.10.

The Chips JU will process personal data in accordance with Regulation (EU) 2018/1725 on the protection of natural persons with regard to the processing of personal data by the Union institutions, bodies, offices and agencies and on the free movement of such data, and repealing Regulation (EC) No 45/2001 and Decision No 1247/2002/EC9.

Once the coordinator (or sole applicant) has submitted an application, an acknowledgement of receipt will be sent by the JU. No other interaction will take place with the Chips JU until the application has been evaluated, unless the Chips JU needs to contact you (usually through the coordinator) to clarify matters such as eligibility or to request additional information.

END OF THE CALL FOR PILOT LINE DOCUMENT

DESCRIPTION OF THE CALL FOR DESIGN PLATFORM (CDP)

Proposals for the Design Platform will be solicited through a Call for Design Platform (CDP).

The document describing the CDP and every facet of this call including the necessary elements for the 2 interrelated calls is included in this chapter and will be used to launch the calls as it contains the details of the procedure.

The Call for Design Platform will merge the technical description of the topic and specific budgets given in Chapter 2, Section 2.4 with the Call Document in this chapter. The Annexes mentioned in this chapter are collected at the end of this chapter.

Call text

Chips Joint Undertaking

REF: Chips-2024-CDP-1

CALL FOR DESIGN PLATFORM

4. INTRODUCTION

4.1. Legal framework

The Chips Joint Undertaking (hereinafter "Chips JU") is established by Council Regulation (EU) 2021/2085 establishing the Joint Undertakings under Horizon Europe[57] (hereinafter "SBA") and modified by an amendment, Council Regulation (EU) 2023/1782 of 25 July 2023[58].

The Chips for Europe Initiative is established under Regulation (EU) 2023/1781 of 13 September 2023[59] (hereinafter "Chips Act"). One objective of the Chips Act is to ensure the conditions necessary for the competitiveness and innovation capacity of the Union. In this context, the Chips for Europe Initiative (the 'Initiative') established by the Chips Act shall promote capacity building to enable design, production and systems integration in next-generation semiconductor technologies.

The Design Platform is one of the components of the Initiative. Concretely, the Initiative will support actions to build a virtual design platform that is available across the Union. The virtual design platform should connect the communities of design houses, start-ups, SMEs and IP and tool suppliers and research and technology organisations to provide virtual prototype solutions based on co-development of technology.

The above is further defined in Article 3 ("Establishment of the Initiative"), Article 4 ("Objectives of the Initiative") and Article 5 ("Content of the Initiative") of the Chips Act. Article 4(2)(b) makes reference to "operational objective 1" which mentions "*building up advanced design capacities for integrated semiconductor technologies".* Article 5(a) further

57 OJ L 427, 30.11.2021, p. 17–119.

58 OJ L 229, 18.9.2023, p. 55–62.

59 OJ L 229, 18.9.2023, p. 1–53.

specifies the content of this operational objective on pilot lines, namely that "*the Initiative shall, under its operational objective 1*:

(i) build up and maintain a virtual design platform, available across the Union, integrating existing and new design facilities with extended libraries and electronic design automation (EDA) tools;

(ii) extend the design capabilities by fostering innovative developments, such as open-source processor architectures and other innovative architectures, chiplets, programmable chips, new types of memory, processors, accelerators or low power chips, that are built in accordance with security-by-design principles;

(iii) enlarge the semiconductor ecosystem by integrating the vertical market sectors, such as health, mobility, energy, telecommunications, security, defence and space, contributing to the green, digital and innovation agendas of the Union.

Article 12(1) of the Chips Act entrusts the implementation of the Initiative's operational objectives 1-4 to the Chips JU. Therefore, operational objective 1 on the Design Platform will be implemented by the Chips JU.

4.1.1. Budget

The Chips JU proceeds to the implementation of the coordinating consortium of the Design Platform which will be fully financed by the Union. The Chips JU shall be tasked with providing financial support, through any instrument or procedure provided for in the Digital Europe Programme[60] (hereinafter "DEP").

In accordance with recital (6) of the SBA Amendment, throughout the lifetime of the Chips Joint Undertaking, up to EUR 2,875 billion shall be dedicated to the Initiative. Of that amount, EUR 1,450 billion shall be for capacity-building activities for operational objectives 1 to 4 and EUR 1,425 billion shall be for research and innovation activities related to operational objectives 1 to 4.

4.1.2. Context and background

4.1.2.1.Rationale

For Europe to sustainably reach its Digital Decade target of 20% market share in semiconductors, and to attract more manufacturing facilities, more chip design activities are required. A critical mass of fabless semiconductor companies is key to generate demand that would justify further investment in semiconductor manufacturing capacity in Europe.

To this end, this initiative will build a pioneering platform, designed to democratise access to cutting-edge chip design technologies. The Design Platform shall serve as a catalyst for the cultivation and expansion of a chip design ecosystem in Europe. By providing centralised tools,

60 Regulation (EU) 2021/694 of 29 April 2021 establishing the Digital Europe Programme and repealing Decision (EU) 2015/2240

resources and support, the Design Platform aims to inspire innovation and propel competitiveness in Europe's semiconductor industry. It will facilitate equal opportunities for innovation across the industry, enabling both small and large entities to drive technological progress, thereby strengthening Europe's position in the global semiconductor market.

4.1.2.1.The Design Platform in the Chips Act

The European **Chips Act** emphasises how fostering the growth of chip design in Europe is a priority, vital for boosting the competitiveness of the European Union's semiconductor industry. The **Design Platform** is at the heart of Pillar 1 of the Chips Act, serving as an interface and entry point to the other activities of the Chips for Europe Initiative. It is envisaged as the key instrument to foster the development of a strong design ecosystem in Europe, by creating a pipeline of highly innovative European fabless companies (particularly start-ups and SMEs). Furthermore, the Design Platform shall enable users to prototype and eventually manufacture their designs at leading foundries.

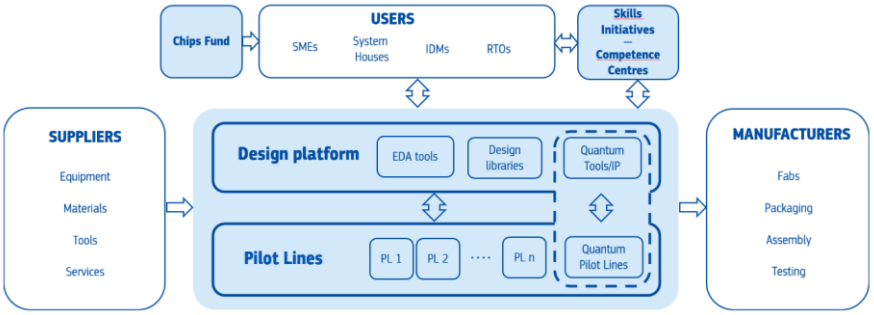


Figure 1 - Chips for Europe Initiative and the Design Platform

As seen in *Figure 1* above, the Design Platform is expected to complement the various **pilot lines** under the initiative by allowing physical prototyping of cutting-edge design on the Platform and direct contact with the Research and Technology Organisations (RTOs) running this infrastructure. This would allow users to experiment with advanced technologies in their design and to fabricate, evaluate and test their first prototypes on the pilot lines. By making the Process Design Kits (PDKs).[61] of the pilot lines and foundries available on the Design Platform, European innovative fabless start-up/SMEs have a lower barrier of entry to chip prototyping and manufacturing. New design tools and libraries for the development of photonics integrated circuits and **quantum chips** shall also be within the scope of the Design Platform.

Furthermore, the Design Platform shall serve as a vital resource for equipping the semiconductor **Competence Centres** in each Member State with the required resources for supporting local companies wishing to engage in chip design.

61 A PDK, is essentially a toolkit that chip designers use when they want to create circuits tailored for a specific manufacturing process of a foundry. By using a PDK, designers ensure that their electronic designs are compatible with the manufacturing technologies at a semiconductor fabrication plant.

4.1.2.2.Overall implementation model

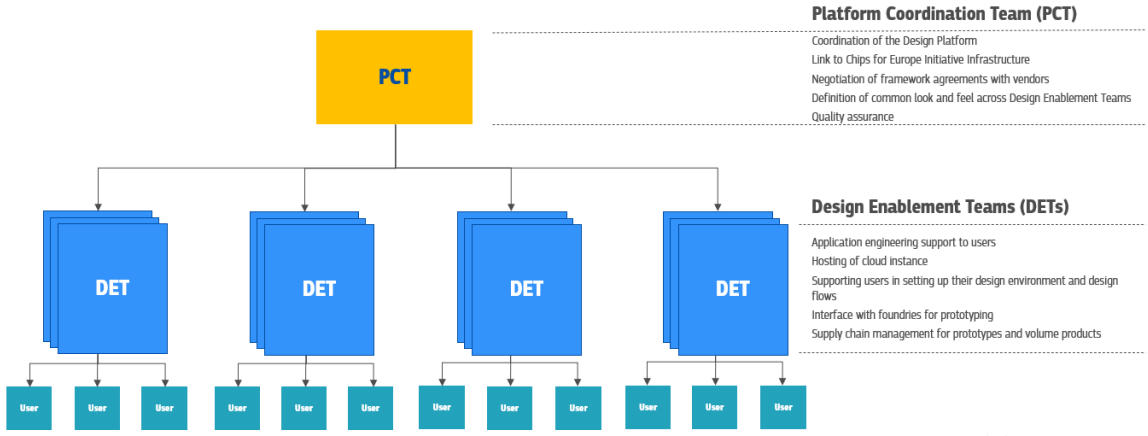


Figure 2 - Implementation model of the Design Platform

The proposed model of implementation depends on a central consortium, referred to as the ***Platform Coordination Team*** (PCT) that operates the overall Design Platform initiative, manages the development of its users and maintains the central cloud service. This service shall be owned by the Chips Joint Undertaking and run by the PCT. It shall consist largely of virtual repositories that shall make EU-funded design assets such as open-source IP and EDA tools widely available to users all across Europe. Furthermore, the PCT, by leveraging the volume of users on the platform, will manage a number of framework agreements with Electronic Design Automation (EDA) and IP vendors for beneficial conditions for start-ups and SMEs making use of the Design Platform, e.g. transparent and advantageous contractual terms for pay-per-use licenses. It is expected that the consortium shall be made up of neutral entities such as Research and Technology Organisations (RTOs).

This model is inspired by EUROPRACTICE, a programme that has been running for 35 years, operated by a number of European RTOs, serving the needs of over 600 academic institutions in chip design training, prototyping, and EDA and IP licensing. The Design Platform shall in turn be targeted towards commercial enterprises, particularly start-ups and SMEs. The first call of the Design Platform should aim to select the consortium that will operate as the PCT and as hosting entity for the platform.

The above is then complemented by a number of decentralised teams referred to as Design Enablement Teams (DETs) that shall set-up a cloud-based environment for users designing on the platform and support them in their design cycle. Furthermore, the DETs shall be responsible for providing access to foundry services. In fact, it shall be a pre-requisite that for an entity to become a DET, it must act as, or be linked to a foundry aggregator.[62]

These DETs shall be design houses and RTOs with the necessary expertise and experience in providing such services. They can be spread geographically but may also have different

62 A foundry aggregator is an industry standard term used for companies that act as an intermediary between fabless semiconductor companies (clients) and semiconductor foundries (manufacturers). Typically, only large enterprises directly engage with foundries.

sectoral (e.g. defence) or technological (e.g. digital, analogue, photonics) focus. The selection of DETs shall take place via an open and inclusive process, based on fulfilment of certain technical and security requirements. Any design service provider fulfilling such requirement may apply for integration into the platform.

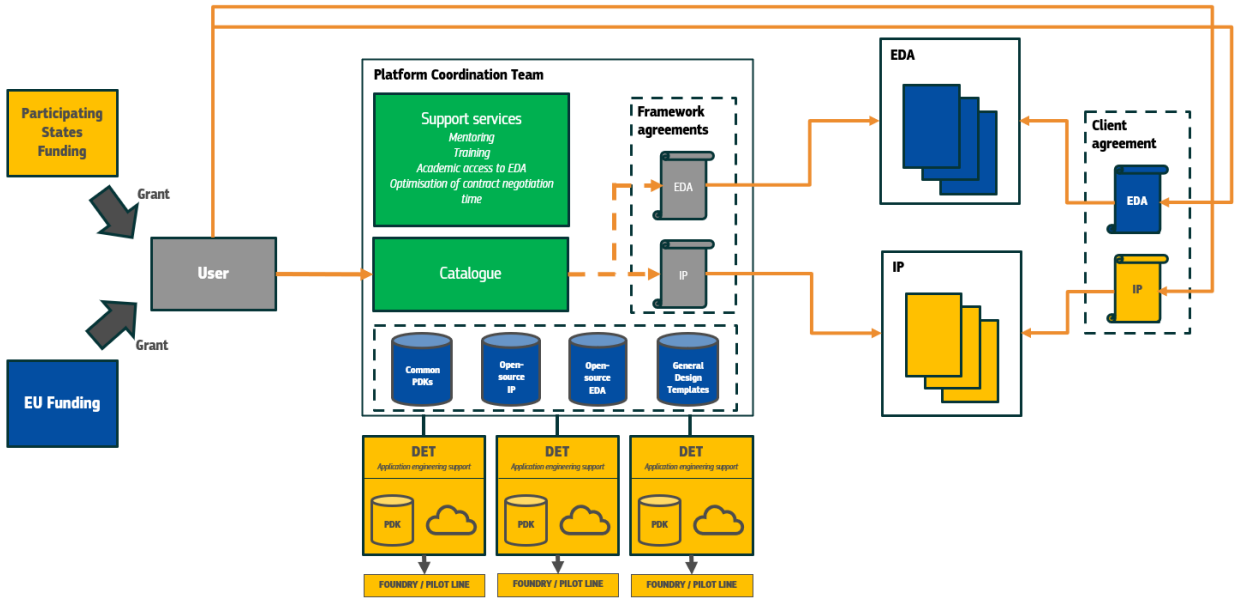


Figure 3 - Design Platform implementation model

The implementation model above balances the need for a centralised and coherent initiative with the importance of ensuring that user companies can have a design environment and local support that suits their needs. As seen in *Figure 3*Figure 3, this approach accommodates the vast array of possible combinations in a design environment, which vary according to technology, design type, and individual company preferences.

Ownership of the cloud-service will lie solely with the Chips JU, with operational support from the PCT within the context of a hosting agreement. The PCT shall assist the Chips JU in defining the technical specifications of the system to be procured. Following the procurement procedure, the PCT shall oversee the operation of the cloud platform, in close cooperation with the organisation selected for the overall integration of the system.

4.1.3. The overall implementation process

Implementing the Design Platform is a complex endeavour requiring a coordinated effort of a series of calls and procurements.

The overall development of the Design Platform can be outlined in four high-level stages, with the main milestones as follows:[63]

- Phase 1: The selection of the consortium in charge of the overall coordination of the Design Platform, referred to as ***the Platform Coordination Team*** (PCT); the definition

63 The different phases of development and timing are indicative. Consortia may propose justified deviations to this timeline. Phases are not necessarily sequential and may be run in parallel.

of technical specifications for the procurement of the cloud service and call for Design Enablement Teams (DETs), and the launch of the project

- Phase 2: Following the definition of the relevant technical specifications in Phase 1, launch of the procurement process for the cloud service and the call for DETs.
- Phase 3: Integration of all components i.e. cloud service, design assets, DETs and other relevant elements and the operationalisation of the platform. Formal launch of the platform, with availability of the cloud service on a 24/7 basis.
- Phase 4: The potential launch of a scheme to support start-ups and SMEs making use of the Platform.[64]

4.1.3.1.The Hosting Consortium

A PCT consortium needs to include:

c) at least one independent legal entity established in a Member State; and
d) at least two other independent legal entities each established in different Participating States.[65]

Furthermore, the PCT consortium in its role as a 'Hosting Consortium', will be composed of one or more Hosting Entities (i.e., entities that **are responsible** for the management of the Design Platform cloud service to be procured by the Chips JU) and possibly other members (i.e., members that **are not responsible** for the management of the Design Platform cloud service to be procured by the Chips JU). One of the consortium members acts as the coordinator; typically, but not necessarily, the coordinator is a Hosting Entity. The coordinator will be mandated by the Hosting Consortium to act on behalf of the other members of the consortium (e.g., to sign the Hosting Agreement – see Annex 2).

A consortium including Hosting Entity(ies) will be selected for managing and maintaining the Design Platform, in collaboration with the selected service provider of the cloud service. The consortium will have as **main responsibilities**:

- to assist the Chips JU in the procurement of the cloud service of the Design Platform;
- to manage and maintain with the selected service provider the cloud service of the Design Platform;

These responsibilities are to be considered in tandem with the expected activities set out in the technical description in Section 2.4.

64 Subject to a decision of the Governing Board of the Chips Joint Undertaking.

65 It must be noted that entities established in Participating States that are associated countries (i.e., not in a Member State or EEA country) will only receive funding from the Programme (HE and/or DEP) their countries are associated to.

4.1.3.2. The present Call Document

The present Call for Design Platform includes two interrelated calls:

- A **Call for Expression of Interest** (hereinafter "CfEoI") for the selection of a Hosting Consortium. Provided certain conditions are fulfilled by the Hosting Entity(ies) of the Hosting Consortium, this CfEoI will entitle the selected Hosting Entity(ies) to manage the procurement of the infrastructure to be acquired under a procurement agreement.
- A **Call for proposals for coordination of the Design Platform,** grant funded under the Digital Europe Programme. The winning consortium would thus become the Platform Coordination Team (PCT). The type of action is a Coordination and Support Action (CSA).

In practice, to cover the activities needed for a PCT, consortia would submit two proposals, one for each of the abovementioned calls. Each call will have its specific admissibility requirements and eligibility, exclusion, and evaluation criteria, as outlined in this document. Consortia submitting proposals to the call for proposals may be different from Hosting Consortia submitting proposals for the Call for Expression of Interest as long as admissibility requirements and eligibility and exclusion criteria of the funding programmes concerned are respected.

These two calls will close on the same date.

At a later stage, in line with any relevant provisions of the Call for Expression of Interest and as part of the coordinating responsibility of the hosting consortium, other related calls may be published, and can include:

- a Call for Tenders, for the procurement of the cloud services and their maintenance;
- one (or more) Call(s) for Proposals for Design Enablement Teams, to support the deployment of chip design cloud-based environments and provide specialised user support;
- a programme to financially support the design costs of start-ups and SMEs through European and national funding.

A tentative timeline for upcoming calls and major milestones is as follows[66]:

Phase	Time	Description
Phase 1	July 2024	Call for Design Platform (*this call*)
	February 2025	Hosting agreement and Grant agreement signature
	March 2025	Start of process leading to the definition of specifications for cloud services

66 The timeline is purely indicative and subject to change and to the discretion of the Chips Joint Undertaking Governing Board. Applying consortia may propose more ambitious timelines.

Phase	Time	Description
		Start of process leading to the definition of requirements for DETs
Phase 2	June 2025	Launch of call for tenders for cloud services
		Launch of call for proposals for DETs
Phase 3	January 2026	Start of integration of all components and the operationalisation of the platform.
Phase 4[67]	September 2026	Potential launch of the platform and support to start-ups and SMEs, to be complemented by contributions from Participating States.

Together with the present Call Document, the following documents[68] are published:

Annex 1	Application form template
Annex 2	Draft Model Hosting Agreement
Annex 5	DEP model grant agreement for coordination of the Design Platform

4.1.3.3. Submission of an application to the present Call Document

Applicants are invited to submit their applications in response to this Call Document by duly completing the application form attached as **Annex 1 to this Call Document**. The application should serve as:

- An expression of interest to be submitted to the Call for Expression of Interest for the selection of a Hosting Consortium for the Design Platform
- A proposal to be submitted for the Call for Proposals for coordination of the Design Platform (Digital Europe Programme, Coordination and Support Action)

67 Phase 4 can start in parallel to phase 3.

68 Some of these documents are drafts. After the opening of the Call, updated drafts may be published on the website of the Chips JU. The final content of these drafts may be agreed upon together with the relevant signatories.

The expression of interest for the selection of a Hosting Consortium will be evaluated by a group of independent experts[69] in accordance with the evaluation criteria set out in Section 4.8.

The call for proposals for coordination of the Design Platform shall be evaluated following the standard methodology for Digital Europe Programme proposals and in line with the criteria set out in Section 4.6.

The result of any evaluation in the context of this Call for Design Platform will be ranked lists.

4.1.3.3.1. Grant under the Digital Europe Programmes

The present call document includes one call for proposals for grants:

→ **A Grant for the operational activities**: this Coordination and Support Action (CSA) grant would cover the coordination and operational activities of the pilot line, i.e., the standard operating costs of the Design Platform. This grant will be established as a Digital Europe Programme Grant Agreement and will be evaluated according to the Digital Europe Programme rules (See Section 4.8.).

Applicants must justify that no double funding is requested. Funding can only be provided on the condition that the prohibition on double funding is respected.

The proposals submitted to each of the inter-related calls and included in the application will be evaluated separately, possibly by the same group of independent experts.

EU funding rates are up to 100% for Coordination and Support Action (CSA) grants under the Digital Europe Programme.

4.1.3.4.The Hosting Agreement

On the basis of the abovementioned ranked lists, the Public Authorities Board (PAB) of the Chips JU will:

- Select the PCT in its role as a Hosting Consortium that will implement the Design Platform;
- Award the grant for ‘coordination of the Design Platform’;

A proposal needs to have passed the applicable thresholds in both evaluations to be selected as the Hosting Consortium and to be awarded the above grants.

69 The group of independent experts that will evaluate the expression of interest for the selection of a Hosting Consortium may be the same group that evaluates the proposals for the Digital Europe Programme call.

Subsequently, the coordinator and the Chips JU will sign a ***Hosting Agreement.*** The Hosting Agreement is the contract that lays down the rules that shall apply to the Hosting Consortium in the context of the implementation of the Design Platform, particularly when it comes to the management and maintenance of the central cloud service. The Hosting Agreement and the conditions described therein are valid until the end of 2031 and may be renewed subject to additional funding under the next MFF.

The obligations of the Hosting Consortium stemming from the Hosting Agreement shall complement the obligations stemming from the Digital Europe Grant Agreement.

However, before the signature of the Hosting Agreement (but after the selection of the Hosting Consortium by the PAB), the Chips JU and the Hosting Consortium may address and finetune elements of the application. The final version agreed upon by the Chips JU and the Hosting Consortium will be the "Description of Action" which will be annexed to the Hosting Agreement and to the Grant Agreement.

4.1.3.5. Responsibility and liability of the consortium

All members of a selected consortium are jointly responsible for their role as the Platform Coordination Team of the Design Platform in line with the Hosting Agreement. In the execution of this action, the consortium is required to establish and implement the necessary internal arrangements.

4.2. OBJECTIVES

The overall objective of the present Call Document is to select a Hosting Consortium in order to implement the Design Platform in line with Section 4.1.3.

The Design Platform to be implemented is described below. The below description should be read in tandem with Section 2.4, Chapter 2.

The semiconductor circuit design process is integral to creating integrated circuits (ICs) and capturing value within the semiconductor value chain. The industry is trending towards more complex, application-specific semiconductors, making advanced design capabilities crucial for competitiveness, particularly in areas like Artificial Intelligence, 5G/6G, wide bandgap semiconductors and the Internet of Things (IoT). Fabless companies, which design chips but outsource manufacturing, play a pivotal role in driving technological advancements and meeting diverse application needs.

The European Chips Act emphasizes the need to grow chip design capabilities in Europe to enhance the competitiveness of the EU's semiconductor industry. The Design Platform is central to this initiative, aiming to build a robust ecosystem of fabless companies, particularly start-ups and SMEs, which currently constitute a small fraction of the global market.

To achieve this objective, this call seeks to designate a Platform Coordination Team (PCT), which shall function as a hosting consortium for the central cloud service to be procured by the Chips JU. The PCT shall bear the responsibility of operating the Design Platform, **managing the associated cloud service**, potentially through the service of a system integrator as procured by the Chips Joint Undertaking, and providing support for user development. Furthermore, the PCT shall assist the Chips Joint Undertaking (Chips JU) in the formulation of technical specifications for Design Enablement Teams and the procurement of the central cloud service of the Design Platform.

The high-level objectives of the designated consortium are:

- **Foster a Strong Design Ecosystem:** Develop a pipeline of innovative European fabless companies to drive technological advancements and competitiveness.
- **Manage and maintain the central Cloud Service**: Manage and maintain the central cloud service as described in Annex B.
- **Democratise access to Electronic Design Automation (EDA) Tools:** Lower barriers for entry by providing access to advanced design tools and resources through a unified cloud-based platform.
- **Support start-ups and SMEs:** Ensure these entities have access to top-tier tools and support services, helping them to innovate and compete on a global scale.
- **Enhance Innovation and Reduce Time-to-Market:** Facilitate rapid development and deployment of chip designs, accelerating the time from concept to market.
- **Facilitate access to the Chips for Europe Initiative infrastructure**: Through for example the provision of pilot line PDKs/ADKs.
- **Set up a network of Design Enablement Teams**: Assist the Chips JU in the upcoming calls for DETs and coordinate their network once DETs are in place.

The target user base shall be primarily commercial entities, especially start-ups and SMEs, engaged in pre-competitive activities such as research, development, and innovation up to prototyping and prior to tape-out. These entities will eventually transition to regular commercial agreements post tape-out. All activities conducted under the Design Platform shall be in compliance with the access conditions set out in Section 2.4.5.

4.2.1. Description of the Design Platform

The technical description of the Design Platform is given in Section 2.4 in the Work Programme part above.

4.3. BUDGET AVAILABLE

The Union financial contribution to the Chips JU for the coordination of the Design Platform shall cover up to 100 % of its total cost.

The total maximum EU budget is as follows:

- Coordination activities: up to EUR 25 million from the Digital Europe Programme.

The Executive Director may adapt the amounts for the actions set out in Section 4 based on the amounts requested in the submissions received.

4.4. CONTENT OF THE APPLICATION

An application must be submitted using the application form included as Annex 1 to this call. As indicated above, the application should include:

- An expression of interest for the Call for Expression of Interest for the selection of a Hosting Consortium for the Design Platform;
- A proposal for the Call for Proposals (CfP) for the coordination of the Design Platform (Digital Europe Programme).

In this application, the consortium must also clearly outline its role as a hosting entity, in accordance with the obligations related to the procured cloud service as detailed in the Technical Description in Section 2.4.

To this end there are two key elements that need to be considered in an application: (i) General provisions; (ii) hosting provisions.

The application needs to contain the following information, amongst other potential considerations:

4.4.1. General provisions

- **Detailed description and timeline**: An overview of the coordination and operational activities of the Platform Coordination Team, with details on the phased implementation approach of the project. Furthermore, the proposal shall include a description of the major phases of the Design Platform's development.

- **Collaboration**: The Platform Coordination Team shall make an effort to have spill-overs beyond its immediate scope and involve a number of relevant stakeholders from across the Union and beyond.
  - Collaboration with other activities under the Chips for Europe Initiative: by ensuring complementarity and, where possible, identify methods of synergy of activities. The application must include a clear overview of the links to the broader Chips for Europe Initiative activities, such as pilot lines, competence centres, and skills development.
  - Collaboration with IP and Electronic Design Automation (EDA) tool vendors: by ensuring effective partnerships with relevant vendors, the Platform Coordination

Team can extend the services it provides to its users. Applicants must propose methods to streamline the licensing process for commercial EDA tools and IP libraries while also considering open-source alternatives.

- **Management of the consortium**: The proposal needs to clearly explain the terms of collaboration between the different members of the consortium and shall provide a credible description of how the various members of the consortium will work in synergy together as a *Platform Coordination Team* in an efficient manner that enables European added value.

- **Business model**: A description of the business model related to the functioning (i.e., service provisioning) of the Design Platform, once it has been set up. Furthermore, if relevant, the business model must outline any potential revenues and how this would contribute to the operations of the Design Platform.

- **Access conditions**: Detailed description of the access conditions to be applied by the Design Platform based on the boundary conditions set by the legal acts, in various parts of the work programme including in Section 2.4. Furthermore, following Article 128(5) SBA Amendment, applicants are reminded of the following guiding principles:
  - Inclusivity: access to the facilities, resources, and expertise related to the Design Platform should be available to a diverse range of users across the European Union. This inclusivity extends to stakeholders from academia, industry, research institutions, and any other entities that are interested in the Design Platform.
  - Transparency: Information regarding the criteria, processes, and terms governing access to the Design Platform shall be clear and transparent to ensure that potential users have a comprehensive understanding of the access framework.
  - Non-Discrimination: Access shall be granted on a non-discriminatory basis, avoiding preferential treatment of potential users based on their geographic location, affiliation, etc.

Furthermore, the following provisions need to be catered for:

- Recognising the role played by start-up and Small and Medium-sized Enterprises (SMEs) in driving innovation and economic growth, the Hosting Consortium must highlight how it intends to support this crucial sector via the Design Platform. To this end, the Hosting Consortium must propose a startup support programme, in line with Annex C, the technical description in section 2.4 and the services and access conditions set out in section 2.4.5.
- Access to the Design Platform needs to take into account EU added value, i.e. contribution to the objectives of the Chips Act as set out in Article 4, as well as economic security considerations.
- Applicants need to anticipate potential situations of excessive demand for access to

the Design Platform, putting in place mechanisms to ensure fairness, transparency, and equal opportunity for all interested parties. The proposal needs to establish clear procedures for managing and mitigating excessive demand, which may include collaboration with external partners, expansion of capacity where feasible, etc.

- The Hosting Consortium must highlight detailed measures to reduce barriers and burdens for companies engaging in chip design.

- **Operational activities**: A description of the activities related to the operation of the Design Platform, the expected engagement with third parties and an estimate of the costs and possible funding required for the satisfactory operation and use of the common infrastructure. The proposal needs to contain a business model that considers any potential revenues based on appropriately defined access conditions, in line with the access conditions described in Section 2.4.5, explaining how such revenues, **if any**, can cover part of the Design Platform's operational expenses. Applicants must provide a detailed description of the proposed management scheme for the Design Enablement Teams. Additionally, proposals should include a comprehensive overview of how the platform can evolve and scale to accommodate increasing demand and technological advancements over time.

- **Budget**: A detailed line-by-line breakdown of all costs related to the coordination of the Design Platform including the operational costs. The proposal must include a distribution of the budget for the three categories over time, with a planning horizon of at least 3 years.

4.4.2. Hosting provisions

The consortium must describe clearly how it intends to follow through on its obligations as a hosting consortium, including:

- **Management of European infrastructure**: A description of the proposed management and maintenance of a cloud-based repository for the designers' community in collaboration with the system integrator selected by the Chips JU following a Call for Tender. Identify and propose the type of design assets to be included, such as open-source IP blocks, design templates, PDKs, open-source tools, and reusable design elements.

- **Curation of repositories**: An overview of how the consortium intends to curate the repositories hosted on the cloud service procured by the Chips JU.

- **User support**: A comprehensive overview on how users shall be supported when making use of the Design Platform's cloud service.

- **Relations with the contracted system integrator**: A description of how the Hosting Consortium intends to organise and manage its relationship with the chosen system integrator for the implementation of the cloud-based service. This shall include

considerations related to service improvement, type of services offered, regular monitoring and cybersecurity. A separate service level agreement between the Hosting Consortium and the chosen system integrator shall be put in place.

The points listed above are not exhaustive. Applying consortia may add other elements to the application as seen appropriate.

4.5. ADMISSIBILITY REQUIREMENTS

An application for the call for Design Platform is not admissible if it has not been introduced under the two calls.

There are no page limits for the application but the consortia are encouraged to limit the narrative part of the application to 200 pages excluding the tables that are expected.

4.5.1. Admissibility requirements for the Call for Expression of Interest

To be admissible:

a) An application must be submitted no later than the **10 October 2024 at 17:00:00 Brussels time.**
b) An application must be submitted electronically (see section "Procedure for the submission"), using the application form in the Annex 1 (Chips JU Application Form)
c) An application must be submitted as described in Section 4.11;
d) The application is written in English.

Failure to comply with those admissibility requirements will lead to the rejection of the application.

4.5.2. Admissibility requirements for the Call for Proposals for the coordination of the Design Platform

Proposals must be submitted before the call deadline **10 October 2024 at 17:00:00 Brussels time.**

Proposals must be complete and contain all the requested information and all required annexes and supporting documents and follow the Application Form.

At proposal submission, the coordinator will have to confirm that it has the mandate to act for all applicants. Moreover, the coordinator will have to confirm that the information in the application is correct and complete and that the participants comply with the conditions for receiving EU funding (especially eligibility, financial and operational capacity, exclusion, etc). Before signing the grant, each beneficiary and affiliated entity will have to confirm this again by signing a declaration of honour (DoH). Proposals without full support will be rejected.

The application must be readable, accessible and printable.

Applicants may be asked at a later stage for further documents (for legal entity validation, financial capacity check, bank account validation, etc).

4.6. ELIGIBILITY CRITERIA

4.6.1. Eligibility criteria for the Call for Expression of Interest

The call is open to entities or consortia of entities fulfilling cumulatively the following conditions:

a) The Hosting Consortium shall include the members that will host and coordinate the Design Platform. Said consortium shall also run the operations of the Platform Coordination Team. The members of the consortium shall be from a Participating State to the Chips JU.
b) A consortium must consist of:
(a) at least one independent legal entity established in a Member State; and
(b) at least two other independent legal entities each established in a different Participating State;
c) The members of the Hosting Consortium shall be registered as a legal entity in one of the Participating States;
The applicant(s) shall have a legal personality on the date of the deadline for submission of applications and must be able to demonstrate their existence as a legal person.

In its application, the coordinator must be given a mandate to represent the other members of the Hosting Consortium to sign and administrate the Hosting Agreement and the various associated grants.

To assess the applicants' eligibility, the following supporting documents are requested:

- The legal entity identification form[70] duly completed and signed by the person authorized to enter into legally binding commitments on behalf of the applicant organization(s) to be submitted in original or a PIC number;

The following entities will be considered as non-eligible:

- natural persons;
- entities without legal personality.

70 http://ec.europa.eu/budget/contracts_grants/info_contracts/legal_entities/legal_entities_en.cfm

4.6.2. Eligibility criteria for the Call for Proposals for the coordination of the Design Platform

Eligible participants (eligible countries)

In order to be eligible, the applicants (beneficiaries and affiliated entities) must:

- be legal entities (public or private bodies)
- be established in one of the eligible countries, i.e.:
  - EU Member States (including overseas countries and territories (OCTs))
  - non- EU countries:
    - EEA countries (Norway, Iceland, Liechtenstein)
    - countries associated to the Digital Europe Programme Specific Objective 6 or countries which are in ongoing negotiations for an association agreement and where the agreement enters into force before grant signature.

Beneficiaries and affiliated entities must register in the Participant Register — before submitting the proposal — and will have to be validated by the Central Validation Service (REA Validation). For the validation, they will be requested to upload documents showing legal status and origin.

Moreover, participation in any capacity (as beneficiary, affiliated entity, associated partner, subcontractor or recipient of financial support to third parties) is limited to entities established in eligible countries.

4.7. EXCLUSION CRITERIA

4.7.1. Exclusion criteria for the Call for Expression of Interest

There are no specific exclusion criteria for the Call for Expression of Interest.

4.7.2. Selection and exclusion criteria for the Call for Proposals for the coordination of the Design Platform

Financial capacity

Applicants must have stable and sufficient resources to successfully implement the projects and contribute their share. Organisations participating in several projects must have sufficient capacity to implement all these projects.

The financial capacity check will be carried out on the basis of the documents applicants will be requested to upload in the Participant Register during grant preparation (e.g. profit and loss account and balance sheet, business plan, audit report produced by an approved external auditor, certifying the accounts for the last closed financial year, etc). The analysis will be

based on neutral financial indicators, but will also take into account other aspects, such as dependency on EU funding and deficit and revenue in previous years.

The check will normally be done for all beneficiaries, except:

- public bodies (entities established as public body under national law, including local, regional or national authorities) or international organisations
- if the individual requested grant amount is not more than EUR 60 000.

If needed, it may also be done for affiliated entities.

If the JU considers that your financial capacity is not satisfactory, it may require:

- further information
- prefinancing paid in instalments
- (one or more) prefinancing guarantees

or

- propose no prefinancing
- request that you are replaced or, if needed, reject the entire proposal.

Operational capacity

Applicants must have the know-how, qualifications and resources to successfully implement the project and contribute their share (including sufficient experience in projects of comparable size and nature).

This capacity will be assessed together with the 'Implementation' award criterion, on the basis of the competence and experience of the applicants and their project teams, including operational resources (human, technical and other) or, exceptionally, the measures proposed to obtain it by the time the task implementation starts.

If the evaluation of the award criterion is positive, the applicants are considered to have sufficient operational capacity.

Applicants will have to show their capacity via the following information:

- general profiles (qualifications and experiences) of the staff responsible for managing and implementing the project
- description of the consortium participants
- list of previous projects (key projects for the last 4 years).

Additional supporting documents may be requested, if needed to confirm the operational capacity of any applicant.

Exclusion

Applicants which are subject to an EU exclusion decision or in one of the following exclusion situations that bar them from receiving EU funding can NOT participate[71]:

- bankruptcy, winding up, affairs administered by the courts, arrangement with creditors, suspended business activities or other similar procedures (including procedures for persons with unlimited liability for the applicant's debts)
- in breach of social security or tax obligations (including if done by persons with unlimited liability for the applicant's debts)
- guilty of grave professional misconduct (including if done by persons having powers of representation, decision-making or control, beneficial owners or persons who are essential for the award/implementation of the grant
- committed fraud, corruption, links to a criminal organisation, money laundering, terrorism-related crimes (including terrorism financing), child labour or human trafficking (including if done by persons having powers of representation, decision-making or control, beneficial owners or persons who are essential for the award/implementation of the grant
- shown significant deficiencies in complying with main obligations under an EU procurement contract, grant agreement, prize, expert contract, or similar (including if done by persons having powers of representation, decision-making or control, beneficial owners or persons who are essential for the award/implementation of the grant
- guilty of irregularities within the meaning of Article 1(2) of EU Regulation 2988/95 (including if done by persons having powers of representation, decision-making or control, beneficial owners or persons who are essential for the award/implementation of the grant)
- created under a different jurisdiction with the intent to circumvent fiscal, social or other legal obligations in the country of origin or created another entity with this purpose (including if done by persons having powers of representation, decision-making or control, beneficial owners or persons who are essential for the award/implementation of the grant).

Applicants will also be rejected if it turns out that[72]:

- during the award procedure they misrepresented information required as a condition for participating or failed to supply that information
- they were previously involved in the preparation of the call and this entails a distortion of competition that cannot be remedied otherwise (conflict of interest).

71 Articles 136 and 141 of Regulation (EU, Euratom) 2018/1046 on the financial rules applicable to the general budget of the Union.

72 See Article 141 of Regulation (EU, Euratom) 2018/1046 on the financial rules applicable to the general budget of the Union.

4.7.3. Rejection from the Call

The Executive Director of the Chips JU shall not conclude a Hosting Agreement with a consortium where:

- Any applicant has misrepresented the information required as a condition for participating in the procedure or has failed to supply that information.

The same exclusion criterion applies to affiliated entities.

Administrative sanctions (exclusion) may be imposed on applicants, or affiliated entities where applicable, if any of the declarations or information provided as a condition for participating in this procedure prove to be false.

4.8. EVALUATION CRITERIA

4.8.1. Evaluation criteria for the Call for Expression of Interest

This Section explains the evaluation criteria for the CfEoI. Eligible applications will be evaluated according to the following evaluation criteria:

1. **Excellence and relevance**
    - *Clarity and pertinence of the proposal vis-à-vis the objectives of the Design Platform, and the extent to which the proposal complies with the general specifications, is ambitious, and is relevant for the Initiative and the other components of the Chips Act.*
    - *Soundness of the proposed methodology, including the underlying concepts, models, assumptions.*
    - *Clarity and pertinence of the cooperation between the Design Platform and the other actions under the Chips for Europe Initiative.*
    - *Clarity and pertinence of access conditions and their practical implementation, including the business plan for operating the Design Platform.*

2. **Impact**
   The extent to which the outputs of the project shall contribute at the European and/or international level to:
    - *Credibility of the pathways to achieve the expected outcomes and impacts, and the likely scale and significance of the contributions.*
    - *Suitability and quality of the measures to maximize expected outcomes and impacts, as set out in the dissemination and exploitation plan, including communication activities.*
    - *Significant spill-overs that support the broader European semiconductor ecosystem.*

3. **Quality and efficiency of the implementation**
   The following aspects will be considered:
    - *Quality and effectiveness of the work plan, assessment of risks, and*

appropriateness of the effort assigned to work packages, and the resources overall.

- *Capacity and role of each participant, and the extent to which the consortium brings together the necessary expertise.*

Experience of the Hosting Entity(ies) in implementing and operating similar systems;

- *Quality and pertinence of experience of the Hosting Entity in chip design related activities and similar initiatives.*
  Extent that provided experience is sufficient for supporting the operation of the Design Platform as described in the Call for Design Platform.

Quality of service to the users, namely capability to comply with the service level agreement provided among the documents accompanying the selection procedure;

- *Quality and pertinence of service to the users, namely capability to comply with the service level agreement provided in the Hosting application.*
- *Quality of the proposed coordination and/or support measures to ensure requested service level towards Design Platform users.*

Overview of the operating cost for the coordination of the Design Platform during its lifetime;

- *Clarity and effectiveness of the estimated cost of implementation of the application.*
- *Appropriateness of the methodology to calculate, report, validate and verify the operating costs.*

Criterion	**Maximum score**	**Threshold**
Excellence and Relevance	30	15
Impact	30	15
Quality and efficiency of the implementation including the Total Cost of Ownership	40	20
	100	60

Points will be allocated out of a total of 100 based on the table. Applications below these thresholds will be rejected.

4.8.2. Evaluation criteria for the Call for Proposals for the coordination of the Design Platform

The award criteria for this call are as follows:

1. Relevance

- Alignment with the objectives and activities as described in section 2.4 and Chapter 4 of

this document.
- Contribution to long-term policy objectives, relevant policies and strategies, and synergies with activities at European and national level

2. Implementation
- Maturity of the project
- Soundness of the implementation plan and efficient use of resources
- Capacity of the applicants, and when applicable the consortium as a whole, to carry out the proposed work.

3. Impact
- Extent to which the project will achieve the expected outcomes and deliverables referred to in this document and, where relevant, the plans to disseminate and communicate project achievements.
- Extent to which the project will strengthen competitiveness and bring important benefits for society.

Evaluation scores will be awarded for the criteria. For full applications, each criterion will be scored out of 5. The threshold for individual criteria will be 3. The overall threshold, applying to the sum of the three individual scores, will be 10. There is no weighting.

Proposals that pass the individual thresholds AND the overall threshold will be considered for funding within the limits of the available budget (i.e. up to the budget ceiling). Other proposals will be rejected.

4.9. OVERVIEW OF THE EVALUATION AND SELECTION PROCEDURE

The Chips JU is responsible for the implementation of the evaluations of the received applications. It organises the submission and evaluation procedures and communicates with the applicants.

The following describes this process. It is the same procedure for the Call for Expression of Interest, as well as for the Call for Proposals for the coordination of the Design Platform.

4.9.1. Evaluation procedure

The submitted applications will be evaluated in a procedure by a panel of seven independent experts. These experts will be appointed by the Chips JU on the basis of the procedure followed under the Digital Europe Programme. This generic procedure to appoint experts will be also used for the Call for Expression of Interest. For the applications considered admissible

according to Section 4.5, the Chips JU will assess the eligibility and exclusion criteria according to Sections 4.6 and 4.7 above. Only admissible and eligible applications will be evaluated.

- **Individual evaluations**: In the first step, the independent experts that sit on the panel shall carry out individually the evaluation of the applications based on the evaluation criteria described in Section 4.8 above. They give a score for each criterion, with explanatory comments. These individual reports form the basis of the further evaluation.
- **Consensus meetings**: After carrying out their individual assessment, all the experts that evaluated the applications shall convene in a consensus meeting, to agree on a common position, including comments and scores and prepare a consensus report. The consensus meetings shall be moderated by a Senior Programme Officer of the Chips JU who shall seek consensus, impartially, and ensure that all applications are evaluated fairly, in line with the relevant evaluation criteria.
- **Panel review**: The review panel shall be chaired by the Executive Director of the Chips JU. The panel will review the scores and comments for all applications to check for consistency across the evaluations. If necessary, it will propose a new set of marks or revise comments, and resolve cases where evaluators were unable to agree. The panel will prepare a final evaluation summary report.

4.9.2. Selection

The Executive Director of the Chips JU will review the results of the evaluation panels and will elaborate final ranking lists for each evaluation, based on the lists proposed by the panels.

This final ranking list shall consist of:

– a main list with the applications to be selected by the experts;

– a reserve list, with applications that have passed the evaluation thresholds.

In addition, the Chips JU will prepare a list with applications that did not pass the evaluation thresholds or were found to be ineligible.

The Executive Director will submit the final ranking lists, together with the Evaluation Summary Reports, to the Public Authorities Board of the Chips JU with a proposal for selection of the application, for approval by the Public Authorities Board.

The Public Authorities Board will make the final selection of consortia whose proposals were selected from submissions to the Call for Expression of Interest for the selection of a Hosting Consortium, and the Call for proposals for the coordination of the Design Platform, funded under the Digital Europe Programme.

After the decision of the Public Authorities Board, all applicants will be informed in writing by the Chips JU of the outcome of the evaluation in the form of Evaluation Summary Reports (ESR). The Chips JU will also inform about the final selection or rejection of applications.

The Chips JU will invite the coordinator of the selected Hosting Consortium to sign a Hosting Agreement with the Chips JU and to initiate grant agreement preparations. The grant agreement will only be concluded subject to the signature of the Hosting Agreement.

4.9.3. Communication

The information contained in the present call document provides all the information required to submit an application. Please read it carefully before doing so, paying particular attention to the priorities and objectives of the present call.

All enquiries must be made by e-mail only to: calls@chips-ju.europa.eu

Questions shall be sent to the above address no later than the **03 October 2024 17:00 Brussels time**, defined as "Deadline to submit questions about the Call" in Section 4.11.

The Chips JU has no obligation to provide clarifications to questions received after this date.

Replies will be given/published no later than the "Publication of the last answers to questions" defined in the timeline in Section 4.10.

To ensure equal treatment of applicants, the Chips JU will not give a prior opinion on the eligibility of applicants, or affiliated entity(ies), an action or specific activities.

No individual replies to questions will be sent but all questions together with the answers and other important notices will be published (FAQ in EN) at regular intervals on the website under the relevant call: https://www.chips-ju.europa.eu/initiative/.

The Chips JU may, on its own initiative, inform interested parties of any error, inaccuracy, omission or clerical error in the text of the Call Document on the mentioned website. It is therefore advisable to consult this website regularly in order to be informed of any updates and of the questions and answers published.

No modification to the applications is allowed once the deadline for submission has elapsed. If there is a need to clarify certain aspects or to correct clerical mistakes, the Chips JU may contact the applicant for this purpose during the evaluation process. This is generally done by e-mail. It is entirely the responsibility of applicants to ensure that all contact information provided is accurate and functioning.

In case of any change of contact details, please send an email with the application reference and the new contact details to calls@chips-ju.europa.eu.

In the case of hosting consortia, all communication regarding an application will be done with the coordinator only, unless there are specific reasons to do otherwise, where the consortium coordinator shall be in copy.

Applicants will be informed in writing about the results of the selection process. Unsuccessful applicants will be informed of the reasons for rejection. No information regarding the award

procedure will be disclosed until the notification letters have been sent to the relevant applicants.

4.10. TIMETABLE

The steps and indicative times for the procedure from publication to expected start of the mandate for the selected Hosting Consortium are in the table below:

Selection of Hosting Consortium milestones	**Date and time or indicative period**
Call Document Publication	
Publication of this Call Document	25-07-2024
Submission of applications	
Calls Deadline	10-10-2024 - 17:00
Application Opening day (open of envelopes with expressions of interest)	
Evaluation	November 2024
Selection by Public Authorities Board	December 2024
Notification of results to applicants	
Signature of the hosting agreement	January 2025
Signature of hosting agreement	
Signature of grant agreements	

This schedule is common to the two interrelated calls: publication, submission, evaluation and selection dates are the same.

The time table for the conclusion of the grant agreements for the DEP calls:

Information on the outcome of the evaluation	Maximum 5 months from the final date for submission
Indicative date for the signing of grant agreements	Maximum 8 months from the final date for submission

4.11. PROCEDURE FOR THE SUBMISSION OF APPLICATIONS

4.11.1. For the Call for Expression of Interest

Applications must be submitted **no later than the 10 October 2024 at 17:00 Brussels time.** Application forms are available at https://www.chips-ju.europa.eu/initiative/.

Applications must be submitted in the correct form, duly completed and dated. They must be submitted in electronic copy on https://www.chips-ju.europa.eu/Form-files/ and signed by the

person authorised to enter into legally binding commitments on behalf of the applicant organisation. The electronic version must contain the pdf versions of the application presented in paper and any other relevant files.

Contact point for any questions[73] is calls@chips-ju@europa.eu.

4.11.2. For the Digital Europe Programme Call

Applications submitted to EU funding & tender portal.

4.11.3. Other submission related comments

All applications will be treated confidentially, as well as any submitted related information, data, and documents. The Chips JU will ensure that the process of handling and evaluating applications is carried out in a confidential manner.

External experts are also bound by an obligation of confidentiality.

Applicants shall avoid taking any actions that could jeopardize confidentiality. They must not attempt to discuss their application with persons they believe may act as expert evaluator for the Chips JU.

Your application shall not contain any information that is 'EU classified' under the rules on security of information in the Commission security rules for protecting EU classified information (see also Classification of Information in DEP projects).

The Chips JU will process personal data in accordance with Regulation (EU) 2018/1725 on the protection of natural persons with regard to the processing of personal data by the Union institutions, bodies, offices and agencies and on the free movement of such data, and repealing Regulation (EC) No 45/2001 and Decision No 1247/2002/EC9.

Once the coordinator (or sole applicant) has submitted an application, an acknowledgement of receipt will be sent by the JU. No other interaction will take place with the Chips JU until the application has been evaluated, unless the Chips JU needs to contact you (usually through the coordinator) to clarify matters such as eligibility or to request additional information.

END OF THE CALL FOR DESIGN PLATFORM DOCUMENT

73 Questions on submission must be sent before the deadline indicated in Section 4.11.

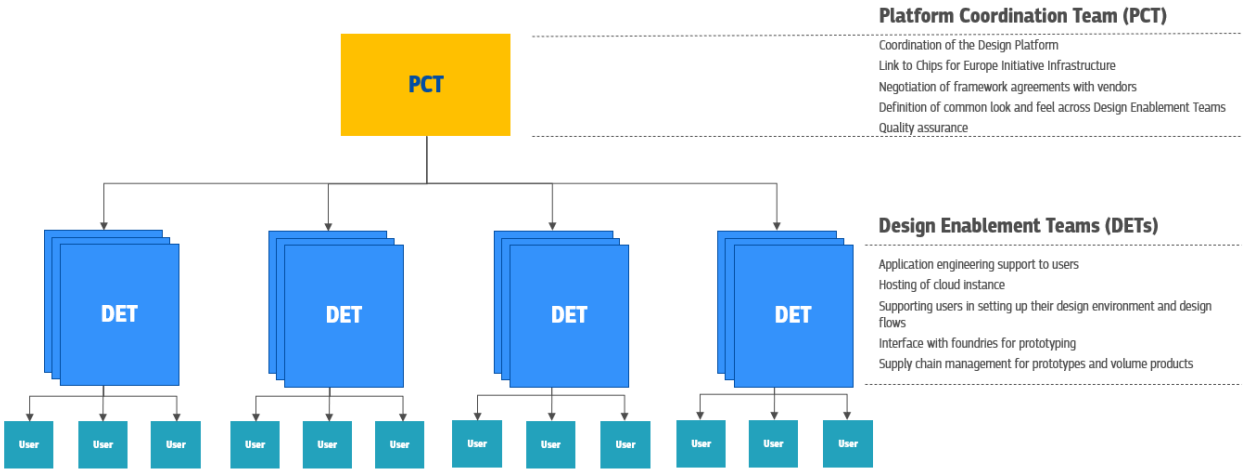
TECHNICAL ANNEXES

Annex A	Design Enablement Teams
Annex B	Cloud services
Annex C	Start-up incubation programme

ANNEXES

Annex I	Letter of Intent for Competence Centre Call
Annex II	General DIGITAL Conditions
Annex III	General Horizon Europe Conditions
Annex IV	Art. 12(6) Regulation (EU) 2021/694
Annex 1	Application form template
Annex 2	Draft Model Hosting Agreement
Annex 3	Draft Model Joint Procurement Agreement
Annex 4	Model Letter of Intent describing the formal commitment of each Participating State (PS) to financially support the pilot line and its participating Consortium members
Annex 5	HE model grant agreement for the R&D activities of the pilot line
Annex 6	DEP model grant agreement for the operational activities of the pilot line

ANNEX A – DESIGN ENABLEMENT TEAMS



A key objective of the Platform Coordination team is to coordinate the Design Platform's various **Design Enablement Teams (DETs)**.

DETs are specialised entities responsible for providing comprehensive, customised support to users throughout their entire chip development process.

The core functions of DETs include, but are not limited to:

1. **Running Electronic Design Automation (EDA) tools on the cloud**: DETs will manage cloud instances from a cloud provider of their choosing,[74] facilitating access to essential design tools and simulation environments.
2. **Design flow support and customisation**: they will assist users in setting up and customising design environments and flows, ensuring smooth progression from initial setup to tape-out.
3. **Application engineering**: DETs will offer dedicated application engineering support, addressing specific user needs and challenges throughout the development process.
4. **Access to Process Design Kits (PDKs)**: users will be provided with access to the necessary PDKs for their design projects.
5. **Prototyping and fabrication services**: DETs will facilitate prototyping and fabrication services through partnerships with leading foundries and the Chips for Europe Initiative pilot lines or other relevant pilot lines.

74 Subject to technical conditions set out by the PCT.

Each DET will manage a cloud instance from a cloud provider of its choosing, and offer dedicated application engineering support to users, from setting up their design environment and design flows to tape-out. The level of security of that cloud instance shall be commensurate to the expected categories of users and applications that are expected to be running on this instance.

It is anticipated that initially around six DETs will be required. DETs can be design houses, RTOs, or other entities interested in providing design enablement services. DETs will be designated based on their technology expertise (e.g. digital, analogue, mixed-signal, etc.), foundry partnerships, and capacity to deliver high-quality services to users, among other characteristics.

These DETs shall be public or private organisations that offer custom design support services, such as ASIC design houses and RTOs, with the necessary expertise and experience in providing such services. All DETs must have credible relationships with foundries or pilot lines as 'foundry aggregators' or equivalent. Overall, the DETs shall cover a wide variety of semiconductor technologies and shall have different sectoral focuses (e.g. automotive, defence).

Disclaimer: Information on Design Enablement Teams is indicative and is without prejudice to potential upcoming calls for Design Enablement Teams.

ANNEX B – CLOUD SERVICES

The PCT is expected to manage cloud services that will be procured by the Chips JU. To this end the PCT shall be involved in the definition of the technical specifications of the eventual procurement.

These cloud services shall primarily contain the following elements:

- A repository populated with an extensive portfolio of open-source and proprietary 'design assets' to facilitate and enhance the design process for users, such as intellectual property (IP) blocks, design templates, fast adoption kits, process design kits (PDKs) from pilot lines and open foundries, open-source design tools, as well as reusable open-access design elements from previous EU-funded projects.
- Any suitable features, such as user authentication and license usage monitoring, that are deemed useful for the management of the overall initiative and the various DETs in the Design Platform.
- Templates of virtual machines or containers containing all the software components and configuration required to operate a given electronic design software, and that can be easily deployed on the cloud instances operated by the DETs.

The latter point shall be complemented by the development of an *Infrastructure as Code* (IaC) framework that supports a variety of cloud vendors. Work related to the development and management of the IaC shall be coordinated by the PCT and deployed across various DETs.

The purpose of this IaC is to facilitate cloud deployment at the various DETs, ensure baseline security standards, and provide a consistent experience across different DETs. Where possible, cloud vendor-agnostic resources shall be used, accompanied by vendor-specific configurations where necessary. The service of developing the IaC shall also be procured by the Chips JU with the technical assistance of the PCT.

The Chips JU may set requirements such as restrictions related to data sovereignty and data transfer in the procurement of the cloud services.

Additional features may be suggested by interested consortia when applying to this call.

Disclaimer: Information on the cloud services is indicative and is without prejudice to potential upcoming calls for tenders launched by the Chips JU.

ANNEX C – START-UP INCUBATION AND ACCELLERATION PROGRAMMES

A key goal of the Design Platform is to overcome a critical barrier in the growth of EU fabless companies: access to funding, ease of access to design tools, computing resources and IP.

Besides the general activities of the Design Platform that are open to all eligible users in line with the access conditions set out in section 2.4., the PCT consortium shall be in charge of running a start-up incubation programme and a start-up acceleration programme in collaboration with the selected DETs.

The **incubation** programme will provide support to early stage start-ups engaged in chip design at Level 1 service of the Design Platform through favourable conditions, which may include access at nominal costs to design tools and IP libraries. The PCT shall define the technical criteria for admission of such start-ups to the incubator programme under the guidance of the Chips Joint Undertaking.

The **acceleration** programme will facilitate the scaling up of start-ups engaged in chip design at Level 2 service of the Design Platform through favourable conditions, which may include vouchers to partially offset operational costs, such as licensing of design tools and IP blocks. The PCT shall coordinate the selection process of these start-ups under the guidance of the Chips Joint Undertaking.

This programme shall be subject to dedicated financial support by the Union and Participating States of the Chips JU.[75]

75 Subject to a decision of the Governing Board of the Chips Joint Undertaking.

ANNEX I: LETTER OF INTENT FOR COMPETENCE CENTRE CALL

Model Letter describing the formal commitment of the Participating State (PS)

Dear Mr Kinaret,
[[[*[Name of authorised representative of the national funding authority or authorities], in representation of [name of the national funding authority] [please indicate as many national funding authorities within the same PS that are involved*]]]

[[[OPTION A (in case in the PS there is one national funding authority funding only one partner of the consortium)
Should the proposal of [name of the partner which will receive funding] be awarded, [name of the national funding authority] will commit the necessary national co-funding of [EUR XXX per year], with a maximum of [EUR XXX] per the duration of the full project, to co-finance the relevant competence centre together with the Union.
*Please note that with this contribution [name of the Participating State] is [providing the same contribution as the maximum Union possible contribution of 1 million euros per year] or [is providing a higher national contribution than the maximum Union possible contribution of 1 million euros per year, acknowledging that this amount shall not lead to a similar higher annual Union contribution] or [is providing a lower national contribution than the maximum Union possible contribution of 1 million euros per year, acknowledging that this will lead to a similar lower annual Union contribution].***]]]**

[[[OPTION B (in case in the PS there is more than one national funding authority providing funding to only one partner of the consortium)
Should the proposal of [name of the partner who will receive funding] be awarded the following national funding authorities will commit the necessary national co-funding, to co-finance the relevant competence centre together with the Union:

- *[Name of national funding authority 1] will commit [EUR XXX per year], with a maximum of [EUR XXX] per the duration of the full project.*
- *[Name of national funding authority 2] will commit [EUR XXX per year], with a maximum of [EUR XXX] per the duration of the full project.*
- *[…]*

Please note that with this contribution [name of the Participating State] is [providing the same contribution as the maximum Union possible contribution of 1 million euros per year] or [is providing a higher national contribution than the maximum Union possible contribution of 1 million euros per year, acknowledging that this amount shall not lead to a similar higher annual Union contribution] or [is providing a lower national contribution than the maximum Union possible contribution of 1 million euros per year, acknowledging that this will lead to a similar lower annual Union contribution].

[[[OPTION C (in case in the PS there is one national funding authority funding more than one partner of the same consortium)**]]]**
Should the proposal of [name of the different partners which will receive funding] be awarded, [name of the national funding authority] will commit the necessary national co-funding of [EUR XXX per year], with a maximum of [EUR XXX] per the duration of the full project, to

co-finance the relevant competence centre together with the Union. This amount will be distributed within the relevant partners as follows:
[Name of partner 1]: [EUR XXX].
[Name of partner 2]: [EUR XXX].
[…]
*Please note that with this contribution [name of the Participating State] is [providing the same contribution as the maximum Union possible contribution of 1 million euros per year] or [is providing a higher national contribution than the maximum Union possible contribution of 1 million euros per year, acknowledging that this amount shall not lead to a similar higher annual Union contribution] or [is providing a lower national contribution than the maximum Union possible contribution of 1 million euros per year, acknowledging that this will lead to a similar lower annual Union contribution].***]]]**

[[[OPTION D (in case in the PS there is more than one national funding authority providing funding to more than one partner of the same consortium)
Should the proposal of [name of the different partners which will receive funding] be awarded the following national funding authorities will commit the necessary national co-funding, to co-finance the relevant competence centre together with the Union:

- *[Name of national funding authority 1] will commit [EUR XXX per year], with a maximum of [EUR XXX] per the duration of the full project. This amount will be committed to fund [name of the partner/s that will be funded including how this amount is distributed per partner]*
- *[Name of national funding authority 2] will commit [EUR XXX per year], with a maximum of [EUR XXX] per the duration of the full project. This amount will be committed to fund [name of the partner/s that will be funded including how this amount is distributed per partner]*
- *[…]*

Please note that with this contribution [name of the Participating State] is [providing the same contribution as the maximum Union possible contribution of 1 million euros per year] or [is providing a higher national contribution than the maximum Union possible contribution of 1 million euros per year, acknowledging that this amount shall not lead to a similar higher annual Union contribution] or [is providing a lower national contribution than the maximum Union possible contribution of 1 million euros per year, acknowledging that this will lead to a similar lower annual Union contribution]. **]]]**

[add text explaining further specificities regarding the national funding authorities' commitments, if needed]

Signature(s) of the authorised representative(s) of the national funding authority(ies)
[…]

ANNEX II: GENERAL DIGITAL EUROPE PROGRAMME CONDITIONS

1. Admissibility

Proposals must be submitted before the call deadline.

Proposals must be submitted **electronically** via the Funding & Tenders Portal Electronic Submission System. Paper submissions are NOT possible.

Proposals (including annexes and supporting documents) must be submitted using the forms provided *inside* the Submission System.

Proposals must be **complete** and contain all the requested information and all required annexes and supporting documents.

- Application Form Part A — contains administrative information about the participants (future coordinator, beneficiaries and affiliated entities) and the summarised budget for the project *(to be filled in directly online)*
- Application Form Part B — contains the technical description of the project *(to be downloaded from the Portal Submission System, completed and then assembled and re-uploaded)*
- Any other mandatory annexes and supporting documents

At proposal submission, you will have to confirm that you have the **mandate to act** for all applicants. Moreover, you will have to confirm that the information in the application is correct and complete and that the participants comply with the conditions for receiving EU funding (especially eligibility, financial and operational capacity, exclusion, etc). Before signing the grant, each beneficiary and affiliated entity will have to confirm this again by signing a declaration of honour (DoH). Proposals without full support will be rejected.

Your application must be **readable**, **accessible and printable**.

You may be asked at a later stage for further documents *(for legal entity validation, financial capacity check, bank account validation, etc).*

For more information about the submission process (including IT aspects), consult the Online Manual.

2. Eligibility

In order to be eligible, the applicants (beneficiaries and affiliated entities) must:

- be legal entities (public or private bodies)
- be established in one of the eligible countries, i.e.:

- EU Member States (including overseas countries and territories (OCTs))
- non-EU countries:
  - listed EEA countries and countries associated to the Digital Europe Programme (list of participating countries)

Beneficiaries and affiliated entities must register in the Participant Register — before submitting the proposal — and will have to be validated by the Central Validation Service (REA Validation). For the validation, they will be requested to upload documents showing legal status and origin.

Moreover, participation in any capacity (as beneficiary, affiliated entity, associated partner, subcontractor or recipient of financial support to third parties) is limited to entities established in eligible countries.

Specific cases

Natural persons — Natural persons are NOT eligible (with the exception of self-employed persons, i.e. sole traders, where the company does not have legal personality separate from that of the natural person).

International organisations — International organisations are not eligible, unless they are International organisations of European Interest within the meaning of Article 2 of the Digital Europe Regulation (i.e. international organisations the majority of whose members are Member States or whose headquarters are in a Member State).

Entities without legal personality — Entities which do not have legal personality under their national law may exceptionally participate, provided that their representatives have the capacity to undertake legal obligations on their behalf, and offer guarantees for the protection of the EU financial interests equivalent to that offered by legal persons[76].

EU bodies — EU bodies (with the exception of the European Commission Joint Research Centre) can NOT be part of the consortium.

Associations and interest groupings — Entities composed of members may participate as 'sole beneficiaries' or 'beneficiaries without legal personality'[77]. Please note that if the action will be implemented by the members, they should also participate (either as beneficiaries or as affiliated entities, otherwise their costs will NOT be eligible).

Countries currently negotiating association agreements — Beneficiaries from countries with ongoing negotiations for participating in the programme *(see list of participating countries above)* may participate in the call and can sign grants if the negotiations are concluded before

76 See Article 197(2)(c) EU Financial Regulation 2018/1046.

77 For the definitions, see Articles 187(2) and 197(2)(c) EU Financial Regulation 2018/1046.

grant signature and if the association covers the call (i.e. is retroactive and covers both the part of the programme and the year when the call was launched).

Following the Council Implementing Decision (EU) 2022/2506, as of 16th December 2022, no legal commitments (including the grant agreement itself as well as subcontracts, purchase contracts, financial support to third parties etc.) can be signed with Hungarian public interest trusts established under Hungarian Act IX of 2021 or any entity they maintain.

Affected entities may continue to apply to calls for proposals. However, in case the Council measures are not lifted, such entities are not eligible to participate in any funded role (beneficiaries, affiliated entities, subcontractors, recipients of financial support to third parties). In this case, co-applicants will be invited to remove or replace that entity and/or to change its status into associated partner. Tasks and budget may be redistributed accordingly.

EU restrictive measures — Special rules apply for certain entities *(e.g. entities subject to EU restrictive measures under Article 29 of the Treaty on the European Union (TEU) and Article 215 of the Treaty on the Functioning of the EU (TFEU)*[78]*)*. Such entities are not eligible to participate in any capacity, including as beneficiaries, affiliated entities, associated partners, subcontractors or recipients of financial support to third parties (if any).

For more information, *see Rules for Legal Entity Validation, LEAR Appointment and Financial Capacity Assessment*.

Ethics

Projects must comply with:

- highest ethical standards and
- applicable EU, international and national law (including the General Data Protection Regulation 2016/679).

Proposals under this call will have to undergo an ethics review to authorise funding and may be made subject to specific ethics rules (which become part of the Grant Agreement in the form of ethics deliverables, *e.g. ethics committee opinions/notifications/authorisations required under national or EU law*).

For proposals involving development, testing, deployment, use or distribution of AI systems, the ethics review will in particular check compliance with the principles of human agency and oversight, diversity/fairness, transparency and responsible social impact, while the experts performing the technical evaluation will assess the robustness of the AI systems (i.e. their reliability not to cause unintentional harm).

Security

78 Please note that the EU Official Journal contains the official list and, in case of conflict, its content prevails over that of the EU Sanctions Map.

Projects involving EU classified information must undergo security scrutiny to authorise funding and may be made subject to specific security rules (detailed in a security aspects letter (SAL) which is annexed to the Grant Agreement).

These rules (governed by Decision 2015/444[79] and its implementing rules and/or national rules) provide for instance that:

− projects involving information classified TRES SECRET UE/EU TOP SECRET (or equivalent) can NOT be funded

− classified information must be marked in accordance with the applicable security instructions in the SAL

− information with classification levels CONFIDENTIEL UE/EU CONFIDENTIAL or above (and RESTREINT UE/ EU RESTRICTED, if required by national rules) may be:

  − created or accessed only on premises with facility security clearance (FSC) from the competent national security authority (NSA), in accordance with the national rules

  − handled only in a secured area accredited by the competent NSA

  − accessed and handled only by persons with valid personnel security clearance (PSC) and a need-to-know

− at the end of the grant, the classified information must either be returned or continue to be protected in accordance with the applicable rules

− action tasks involving EU classified information (EUCI) may be subcontracted only with prior written approval from the granting authority and only to entities established in an EU Member State or in a non-EU country with a security of information agreement with the EU (or an administrative arrangement with the Commission)

− disclosure of EUCI to third parties is subject to prior written approval from the granting authority.

Please note that, depending on the type of activity, facility security clearance may have to be provided before grant signature. The granting authority will assess the need for clearance in each case and will establish their delivery date during grant preparation. Please note that in no circumstances can we sign any grant agreement until at least one of the beneficiaries in a consortium has facility security clearance.

Further security recommendations may be added to the Grant Agreement in the form of security deliverables *(e.g. create security advisory group, limit level of detail, use fake scenario, exclude use of classified information, etc).*

79 See Commission Decision 2015/444/EU, Euratom of 13 March 2015 on the security rules for protecting EU classified information (OJ L 72, 17.3.2015, p. 53).

Beneficiaries must ensure that their projects are not subject to national/third-country security requirements that could affect implementation or put into question the award of the grant *(e.g. technology restrictions, national security classification, etc)*. The granting authority must be notified immediately of any potential security issues.

3. Financial and operational capacity and exclusion

Financial capacity

Applicants must have **stable and sufficient resources** to successfully implement the projects and contribute their share. Organisations participating in several projects must have sufficient capacity to implement all these projects.

The financial capacity check will be carried out on the basis of the documents you will be requested to upload in the Participant Register during grant preparation *(e.g. profit and loss account and balance sheet, business plan, audit report produced by an approved external auditor, certifying the accounts for the last closed financial year, etc)*. The analysis will be based on neutral financial indicators, but will also take into account other aspects, such as dependency on EU funding and deficit and revenue in previous years.

The check will normally be done for all beneficiaries, except:

− public bodies (entities established as public body under national law, including local, regional or national authorities) or international organisations

− if the individual requested grant amount is not more than EUR 60 000.

If needed, it may also be done for affiliated entities.

If we consider that your financial capacity is not satisfactory, we may require:

− further information

− an enhanced financial responsibility regime, i.e. joint and several responsibility for all beneficiaries or joint and several liability of affiliated entities *(see below, section 10)*

− prefinancing paid in instalments

− (one or more) prefinancing guarantees *(see below, section 10)*

or

− propose no prefinancing

− request that you are replaced or, if needed, reject the entire proposal.

For more information, *see Rules for Legal Entity Validation, LEAR Appointment and Financial Capacity Assessment*.

Operational capacity

Applicants must have the **know-how, qualifications** and **resources** to successfully implement the projects and contribute their share (including sufficient experience in projects of comparable size and nature).

This capacity will be assessed together with the 'Implementation' award criterion, on the basis of the competence and experience of the applicants and their project teams, including operational resources (human, technical and other) or, exceptionally, the measures proposed to obtain it by the time the task implementation starts.

If the evaluation of the award criterion is positive, the applicants are considered to have sufficient operational capacity.

Applicants will have to show their capacity via the following information:

- general profiles (qualifications and experiences) of the staff responsible for managing and implementing the project
- description of the consortium participants
- list of previous projects (key projects for the last 4 years; *template available in Part B*).

Additional supporting documents may be requested, if needed to confirm the operational capacity of any applicant.

Exclusion

Applicants which are subject to an **EU exclusion decision** or in one of the following **exclusion situations** that bar them from receiving EU funding can NOT participate[80]:

- bankruptcy, winding up, affairs administered by the courts, arrangement with creditors, suspended business activities or other similar procedures (including procedures for persons with unlimited liability for the applicant's debts)
- in breach of social security or tax obligations (including if done by persons with unlimited liability for the applicant's debts)
- guilty of grave professional misconduct[81] (including if done by persons having powers of representation, decision-making or control, beneficial owners or persons who are essential for the award/implementation of the grant)
- committed fraud, corruption, links to a criminal organisation, money laundering, terrorism-related crimes (including terrorism financing), child labour or human

80 See Articles 136 and 141 of EU Financial Regulation 2018/1046.

81 Professional misconduct includes: violation of ethical standards of the profession, wrongful conduct with impact on professional credibility, false declarations/misrepresentation of information, participation in a cartel or other agreement distorting competition, violation of IPR, attempting to influence decision-making processes or obtain confidential information from public authorities to gain advantage.

trafficking (including if done by persons having powers of representation, decision-making or control, beneficial owners or persons who are essential for the award/implementation of the grant)

− shown significant deficiencies in complying with main obligations under an EU procurement contract, grant agreement, prize, expert contract, or similar (including if done by persons having powers of representation, decision-making or control, beneficial owners or persons who are essential for the award/implementation of the grant)

− guilty of irregularities within the meaning of Article 1(2) of EU Regulation 2988/95 (including if done by persons having powers of representation, decision-making or control, beneficial owners or persons who are essential for the award/implementation of the grant)

− created under a different jurisdiction with the intent to circumvent fiscal, social or other legal obligations in the country of origin or created another entity with this purpose (including if done by persons having powers of representation, decision-making or control, beneficial owners or persons who are essential for the award/implementation of the grant).

Applicants will also be rejected if it turns out that[82]:

- during the award procedure they misrepresented information required as a condition for participating or failed to supply that information

− they were previously involved in the preparation of the call and this entails a distortion of competition that cannot be remedied otherwise (conflict of interest).

82 See Article 141 EU Financial Regulation 2018/1046.

ANNEX III: GENERAL HORIZON EUROPE CONDITIONS

The "Horizon Europe 2023-2025 13. General Annexes (European Commission Decision C(2024)2371 of 17 April 2024)"[83] apply with some exceptions specific to certain calls.

A – Admissibility.

The page limits as mentioned under the different call descriptions in the Chips JU Work Programme 2024 are applicable as well as in the Guide for Applicants regarding the format.

B – Eligibility.

Where eligibility is limited to certain technology readiness levels (TRLs), the table below provides guidance for assessing the TRLs. The table emphasizes the differences between the different levels as well as the difference between hardware and software related actions.

	Definition in HE WP	**Hardware description**	**Software description**	**Exit criteria**
1	Basic principles observed and reported.	Scientific knowledge generated underpinning hardware technology concepts/applications.	Scientific knowledge generated underpinning basic properties of software architecture and mathematical formulation.	Peer reviewed publication of research underlying the proposed concept/application.
2	Technology concept formulated	Invention begins, practical application is identified but is speculative, no experimental proof or detailed analysis is available to support the conjecture.	Practical application is identified but is speculative, no experimental proof or detailed analysis is available to support the conjecture. Basic properties of algorithms, representations	Documented description of the application/concept that addresses feasibility and benefit.

83 Refer to https://ec.europa.eu/info/funding-tenders/opportunities/docs/2021-2027/horizon/wp-call/2023-2024/wp-13-general-annexes_horizon-2023-2024_en.pdf

	Definition in HE WP	Hardware description	Software description	Exit criteria
			and concepts defined. Basic principles coded. Experiments performed with synthetic data.	
3	Experimental proof of concept	Analytical studies place the technology in an appropriate context and laboratory demonstrations, modelling and simulation validate analytical prediction.	Development of limited functionality to validate critical properties and predictions using non-integrated software components., modelling and simulation	Documented analytical/experimental results validating predictions of key parameters.
4	Technology validated in a lab	A low fidelity system/component breadboard is built and operated to demonstrate basic functionality and critical test environments, and associated performance predictions are defined relative to the final operating environment.	Key, functionally critical, software components are integrated, and functionally validated, to establish interoperability and begin architecture development. Relevant Environments defined and performance in this environment predicted.	Documented test performance demonstrating agreement with analytical predictions. Documented definition of relevant environment.
5	Technology validated in relevant environment. (industrially relevant environment in the case of key enabling technologies)	A medium fidelity system is built and operated to demonstrate overall performance in a simulated operational environment with realistic support elements that demonstrates overall performance in	End-to-end software elements implemented and interfaced with existing systems/simulations conforming to target environment. End-to-end software system, tested in relevant environment, meeting predicted performance.	Documented test performance demonstrating agreement with analytical predictions. Documented definition of scaling requirements.

	Definition in HE WP	Hardware description	Software description	Exit criteria
		critical areas. Performance predictions are made for subsequent development phases.	Operational environment performance predicted. Prototype implementations developed.	
6	Technology demonstrated in relevant environment (industrially relevant environment in the case of key enabling technologies)	A high fidelity system/component prototype that adequately addresses all critical scaling issues is built and operated in a relevant environment to demonstrate operations under critical environmental conditions.	Prototype implementations of the software demonstrated on full-scale realistic problems. Partially integrate with existing hardware/software systems. Limited documentation available. Engineering feasibility fully demonstrated.	Documented test performance demonstrating agreement with analytical predictions.
7	System prototype demonstration in an operational environment.	A high fidelity engineering unit that adequately addresses all critical scaling issues is built and operated in a relevant environment to demonstrate performance in the actual operational environment and platform.	Prototype software exists having all key functionality available for demonstration and test. Well integrated with operational hardware/software systems demonstrating operational feasibility. Most software bugs removed. Limited documentation available.	Documented test performance demonstrating agreement with analytical predictions.
8	System complete and qualified	The final product in its final configuration is successfully demonstrated through test and analysis for its intended	All software has been thoroughly debugged and fully integrated with all operational hardware and software systems. All user documentation, training	Documented test performance verifying analytical predictions.

	Definition in HE WP	Hardware description	Software description	Exit criteria
		operational environment and platform	documentation, and maintenance documentation completed. All functionality successfully demonstrated in simulated operational scenarios. Verification and Validation (V&V) completed.	
9	Actual system proven in an operational environment (competitive manufacturing in the case of key enabling technologies, or in space)			

D – Award criteria

Scores and weighting factors are indicated in the calls/topics specific annexes

F - Procedure. Evaluation procedure and ranking.

The call specific annexes contain the rules applicable to the Chips JU call evaluations. The rules for evaluation and selection of proposals, as adopted by the GB (GB 2024.71), include the rules on conflicts of interest. This document is available in the calls pages in the Funding and tenders portal.

G – Legal and financial set-up of the grant agreement.

The call/topic descriptions contain the provisions and funding rates applicable to the calls.

ANNEX IV– ART. 12(6) OF REGULATION (EU) 2021/694.

As indicated in the work programme, for duly justified security reasons, legal entities established in associated countries[84] and legal entities that are established in the Union but are controlled from third countries may be eligible to participate[85] only if they comply with the requirements/conditions indicated below.

EEA EFTA countries are fully associated to the Digital Europe Programme and benefit from a status equivalent to that of the Member States. Other formally associated countries can participate under conditions described below.

The assessment of the foreign control is part of the eligibility criteria. For this, participants will be requested to fill in a self-assessment questionnaire to determine their control status during proposal submission. They will also be requested to submit supporting documents in order for the Commission to determine that the entities are not controlled from a third country.

Entities controlled from a third country and entities from associated countries can participate in topics where Article 12(6) of Regulation (EU) 2021/694 (DEP) applies, provided that they comply with certain conditions set out below. Those participants will be asked for guarantees approved by the eligible country in which they are established. The validity of these guarantees will be later assessed by the Chips Joint Undertaking.

Conditions for foreign controlled entities

The applicants that are established in an associated country and applicants that are established in the Union but are controlled from third countries shall be required to provide information demonstrating that:

a) control over the applicant's corporate structure and decision-making process is not exercised in a manner that restrains or restricts in any way its ability to perform and complete the action;
b) the access by non-eligible third countries or by non-eligible third country entities to classified or non-classified sensitive information[86], such as e.g., know-how and business secrets relating to the action will be prevented;
c) the persons involved in the action will have national security clearance issued by a Member State where appropriate;

84 Participation is further limited to associated countries that meet specific conditions. In order to be eligible, a third country must be formally associated to Digital Europe Programme and meet specific conditions (eligibility depending on the outcome of the assessment of replies to the questionnaire provided by relevant associated countries to meet these specific conditions) at the time of signature of the grant agreement.

85 See Article 12(6) of the Regulation (EU) 2021/694.

86 Commission Decision 2015/444/EC, Euratom of 13 March 2015 on the security rules for protecting EU classified information (OJ L 72, 17.3.2015, p. 53).

d) the results of the action shall remain within the beneficiary and shall not be subject to control or restrictions by non-eligible third countries or other non-eligible third country entities during the action and for a specified period after its completion.
e) For applicants established in the EU and controlled from a third country and established in Associated Countries that they are not subject to export restrictions to EU Member States on results, technologies, services and products developed under the project for at least 4 years after the end of the action, in order to ensure the security of supply.

More information about the procedure, the conditions and the guarantees will be detailed in the call documents and the online manual in the EU Funding & Tenders Portal. Procurement actions will also be subject to Article 12(6) DEP and, when applying this article, will use the same conditions as calls for proposals (a, b and d).