APPENDIX 5: ACTIVITIES LAUNCHED IN 2025 FOR THE ECS PART

Version 2

CONTENTS

1 WORK PROGRAMME 2025: ELECTRONIC COMPONENTS AND SYSTEMS PART

The part of the ECS programme WP2023-2027 foresees the launch of three calls for proposals in 2025. Other operational activities include:

- the start of the projects selected under the Chips ECS calls 2024,
- the monitoring of the projects selected in calls 2021, 2022 and calls 2023,
- the monitoring of the projects selected in the ECSEL JU Calls 2014-2020,
- the preparation of work programme updates for years 2026 and beyond, in particular the focus topics,
- various supporting activities to communication, administration & finance.

To prepare a future call to boost the R&I cooperation between EU and Japan on semiconductors, the Office will launch an Expression of Interest.

2 LAUNCH OF CHIPS JU CALLS ECS PART

The estimated maximum operational budget for the ECS part of the programme of the Chips JU is EUR 231 million for the calls, and an amount of EUR 1 million will be reserved for contracting experts involved in the evaluation of projects and monitoring of the project implementation.

In 2025, the Chips JU will launch four calls for proposals:

- A first call for Innovation Actions (higher TRLs) consists of a global call topic and 2 focus topics, run in 2 stages.
- The second call for Research and Innovation Actions (lower TRLs) and consists of a global call topic, run in 2 stages.
- A third call includes one Coordination and Support Action (CSA) topic that will be implemented as one stage call without national contribution.
- A fourth single-stage call on Heterogeneous integration for high-performance automotive computing.

The two global call topics, on selected chapters of the Strategic Research and Innovation Agenda 2025[1] (hereinafter, "SRIA", aim at the reinforcement of the industrial competitiveness, stimulating industrial innovation and transfer of innovation from research environments (RTOs and Universities) to SMEs and Large Enterprises. Research and Innovation Actions (RIA) and

[1] https://ecssria.eu/2025

Innovation Actions (IA) differ by the Technology Readiness Level (TRL) and therefore by the reimbursement rates.

Projects selected should demonstrate high industrial impact, along the value chain, Europe wide collaboration with a mixed participation of large enterprises, SMEs and academia.

Expected outputs are novel technologies and applications, pilot lines, large scale demonstrators, and platforms for innovative product developments.

3 EU INDICATIVE BUDGET FOR THE CHIPS JU ECS CALLS 2025

Action	**Topic**	**EU indicative budget (M€)**
HORIZON-JU-Chips-2025-IA	**Global call according to SRIA 2024 (IA)**	70
HORIZON-JU-Chips-2025-IA-HIA	**Heterogeneous integration for high-performance automotive computing**	20
HORIZON-JU-Chips-2025-IA FT1	**RISC-V Automotive Hardware Platform**	80
HORIZON-JU-Chips-2025-IA FT2	**AI-assisted Methods and Tools for Engineering Automation**	20
HORIZON-JU-Chips-2025-RIA	**Global RIA call**	40
HORIZON-Chips-2025-CSA	**Boosting R&I cooperation between EU and Japan on semiconductors**	1
	Total	231

4 TECHNICAL DESCRIPTION OF THE CALLS

4.1 ECS GLOBAL IA

Topic: HORIZON-JU-Chips-2025-IA

Type of Action	Innovation Action (IA)
Indicative EU budget	70 M€
Mode	Co-funded with the NFA Two stage Call, with submission of Project Outline (PO) and of Full Proposal (FPP)
Call launch date	04 Mar 2025
Deadline PO	29 Apr 2025 at 17:00 Brussels Time
Deadline FPP Stage	17 Sep 2025 at 17:00 Brussels Time

4.1.1.1 Context

This topic is the IA-part of the bottom-up programming. The topic will be open to the major challenges addressed in the current version of the Chips JU Strategic Research and Innovation Agenda, excluding the topics addressed in the focus topics of all the HE Chips JU calls in 2025 (ECS and Chips for Europe calls).

Aspects of ECS value chain integration are important for the Chips JU programme and the whole European ECS sector, across applications and across capabilities, as well as cutting across disciplines, supporting platform building, interoperability, establishing open standards. The participation of SMEs in the developments allowing them to play effective roles while working on solutions that can be taken exploited by SMEs is important in view of the SBA.

4.1.1.2 Expected Outcomes

A Chips JU Innovation Action (IA) primarily consists of activities aiming at technology or method introduction, pilot lines, test beds, demonstrators, innovation pilots and zones of full-scale testing. These activities produce plans and arrangements or designs for new, altered, or improved products, processes, methods and tools or services. For this purpose, they may include prototyping, testing, demonstrating, piloting, large-scale product validation and market replication.

A ‘technology or method introduction’ aims at the development, testing, and implementation of new technologies, tools or methods, which are a critical element of innovative products, which will be created in subsequent projects.

A ‘demonstration or pilot’ aims to validate the technical and economic viability of a new or improved technology, product, process, service or solution in an operational (or nearly operational) environment, whether industrial or otherwise, involving, where appropriate, a larger scale prototype or demonstrator.

A ‘market replication’ aims to support the first application/deployment in the market of an innovation that has already been demonstrated but not yet applied/deployed in the market due to market failures/barriers to uptake. ‘Market replication’ does not cover multiple applications in the market of an innovation that has already been applied successfully once in the market. ‘First’ means new at least to Europe or new at least to the application sector in question. Often such projects involve a validation of technical and economic performance at system level in real life operating conditions provided by the market.

The activities have their centre of gravity at the TRL 5-8. An IA proposal in Chips JU is characterized by one or more of the following:

- Execution by an industrial consortium that may consist of large enterprises and SMEs but also including universities, institutes, public organizations.
- Using innovative technology
- Establishment of a new and realistic innovation environment connected with an industrial environment, such as:
  - a pilot line facility capable of manufacturing
  - a zone of full-scale testing
  - a development of new processes or tools and their introduction in several domains
  - the development of frameworks or platforms together with the usage of these frameworks or platforms in innovative products.
- Having a deployment plan leading to short to midterm economic value creation in Europe.

To maximize effective implementation of the Chips JU top-level objectives, the list of IA proposals to be retained for public funding should constitute a balanced portfolio of projects developing innovative technologies (as defined in the SRIA in the functional technology layers and cross-sectional technologies sections) and applying them in different domains (as defined in the SRIA in ECS key application areas section). The domains represent the demand side of technologies, and the development of new technologies represents the supply side of technologies.

The size of the proposal is not an evaluation criterion. Chips JU is looking at a balanced portfolio of small and large projects.

4.1.1.3 Scope

The global topic will be open to the following major challenges as defined in the SRIA:

Topics and Major Challenges		Open/Closed
1.1 - Process technology, equipment, materials and manufacturing		
	Major Challenge 1: Advanced computing, in-memory, neuromorphic, photonic, and quantum computing concepts	Open
	Major Challenge 2: Novel sensor, actuation and other devices that enable advanced functionality	Open
	Major Challenge 3: Advanced integration solutions	Open
	Major Challenge 4: Advanced wafer fab equipment and manufacturing solutions	Open
	Major Challenge 5: Advanced packaging, assembly & test equipment solutions	
	Major Challenge 6: Sustainable semiconductor manufacturing	
1.2 - Components, modules and systems integration		
	Major Challenge 1: Functionality	Open
	Major Challenge 2: Advanced Integration solutions	Open
	Major Challenge 3: Heterogenous integration	Open
	Major Challenge 4: Sustainability	
1.3 - Embedded software and beyond		
	Major Challenge 1: Efficient engineering of embedded software	Open
	Major Challenge 2: Continuous integration and deployment	Open
	Major Challenge 3: Lifecycle management	Open
	Major Challenge 4: Embedding data analytics and Artificial Intelligence	Open
	Major Challenge 5: Support for Sustainability by embedded software	Open
	Major Challenge 6: Software reliability and trust	Open

	Major Challenge 7: Hardware virtualization for efficient SW engineering	Open
1.4 - System of Systems		
	Major Challenge 1: Open SoS architecture and infrastructure	Open
	Major challenge 2: SoS interoperability	Open
	Major Challenge 3: Evolvability of SoS composed of embedded and cyber-physical systems	Open
	Major Challenge 4: SoS integration along the life cycle	Open
	Major Challenge 6: SoS monitoring and management	Open
2.1 - Edge Computing and Embedded Artificial Intelligence		
	Major Challenge 1: Increasing energy efficiency	Open
	Major Challenge 2: Managing the increasing complexity of systems	Open
	Major Challenge 3: Supporting the increasing lifespan of devices and systems	Open
	Major Challenge 4: Ensuring European sustainability	Open
2.2 – Connectivity		
	Major Challenge 1: Strengthening the EU connectivity technology portfolio to maintain leadership, secure sovereignty and offer an independent supply chain	Open
	Major Challenge 2: Investigate innovative connectivity technology (new spectrum or medium) and new approaches to improving existing connectivity technology to maintain the EU's long-term leadership	Open
	Major Challenge 3: Autonomous interoperability translation for communication protocol, data encoding, compression, security and information semantics	Open
	Major Challenge 4: Architectures and reference implementations of interoperable, secure, scalable, smart and evolvable IoT and SoS connectivity from edge to cloud	Open
	Major Challenge 5: Network virtualisation enabling run-time and evolvable integration, deployment and management of edge to cloud network architectures	Open
2.3 - Architecture and design: methods and tools		

	Major Challenge 1: Enabling cost- and effort-efficient Design and Validation Frameworks for High Quality ECS. The ever-increasing functionality of ECS, usage and integration of new technologies to enable these functions and the high demands for validation and testing to ensure their quality drive the need for efficient, framework- and tool-supported design and validation processes and frameworks.	Open
	Major Challenge 2: Enabling Sustainable Design for Sustainability. Methods and tools to support the design and validation of sustainable ECS as well as supporting a sustainable design and validation process.	Open
	Major Challenge 3: Managing complexity. This challenge deals with methods to handle the ever-increasing complexity of ECS-based systems.	Open
	Major Challenge 4: Managing diversity. Handling diversity in all aspects of developing ECS-based systems is the key objective of this challenge	Open
2.4 - Quality, reliability, safety and cybersecurity		
	Major Challenge 1: Ensuring HW quality and reliability	Open
	Major Challenge 2: Ensuring dependability in connected software	Open
	Major Challenge 3: Ensuring cyber-security and privacy	Open
	Major Challenge 4: Ensuring of safety and resilience	Open
	Major Challenge 5: Human systems integration	Open
3.1 – Mobility		
	Major Challenge 1: SDV hardware platforms: modular, scalable, flexible, safe & secure	**Closed**
	Major Challenge 2: SW platforms for SDV of the future: modular, scalable, re-usable, flexible, safe & secure, supporting edge2cloud applications	Open
	Major Challenge 3: Green deal: enable climate and energy optimal mobility	Open
	Major Challenge 4: Digitalisation: affordable and safe automated and connected mobility for passengers and freight	Open
	Major Challenge 5: Edge2cloud mobility applications: added end-user value in mobility	Open

	Major Challenge 6: AI enabled engineering tool chain: agile collaborative SDV SW development and SDV as well as ADAS/AD validation	**Closed**
3.2 – Energy		
	Major Challenge 1: Smart & Efficient - Managing Energy Generation, Conversion, and Storage Systems	Open
	Major Challenge 2: Energy Management from On-Site to Distribution Systems	Open
	Major Challenge 3: Future Transmission Grids	Open
	Major Challenge 4: Achieving Clean, Efficient & Resilient Urban/ Regional Energy Supply	Open
	Major Challenge 5: Cross-Sectional Tasks for Energy System Monitoring & Control	Open
3.3 - Digital Industry		
	Major challenge 1: Responsive and smart production	Open
	Major challenge 2: Sustainable production	Open
	Major challenge 3: Artificial Intelligence in digital industry	Open
	Major challenge 4: Industrial service business, lifecycles, remote operations and teleoperation	Open
	Major challenge 5: Digital twins, mixed or augmented reality, telepresence	Open
	Major challenge 6: Autonomous systems, collaborative robotics	Open
3.4 - Health and wellbeing		
	Major Challenge 1: Enable digital health platforms based upon P4 healthcare	Open
	Major Challenge 2: Enable the shift to value-based healthcare, enhancing access to 4P’s game-changing technologies	Open
	Major Challenge 3: Support the development of the home as the central location of the patient, building a more integrated care delivery system	Open
	Major Challenge 4: Enhance access to personalised and participative treatment for chronic and lifestyle-related diseases	Open

	Major Challenge 5: Ensure more healthy life years for an ageing population	Open
3.5 - Agrifood and natural resources		
	Major Challenge 1: Food security	Open
	Major Challenge 2: Food safety	Open
	Major Challenge 3: Environmental protection and sustainable production	Open
	Major Challenge 4: Water resource management	Open
	Major Challenge 5: Biodiversity restoration for ecosystems resilience, conservation, and preservation	Open
3.6 - Digital Society		
	Major Challenge 1: Facilitate individual self-fulfilment	Open
	Major Challenge 2: Facilitate empowerment and resilience	Open
	Major Challenge 3: Facilitate inclusion and collective safety	Open
	Major Challenge 4: Facilitate supportive infrastructure and a sustainable environment	Open

Detailed descriptions of all major challenges can be found in the SRIA.

Aspects of ECS value chain integration are important for the Chips JU programme and the whole European ECS sector, across applications and across capabilities. Consortia are encouraged to submit proposals that take this aspect into account.

Proposals that cut across disciplines, support platform building, interoperability, establishment of open standards are particularly encouraged; even outside the regular ECS sector.

Proposals should encourage SMEs to participate in the developments, in particular paying attention to the needs of SMEs, allocate SMEs effective roles in project execution, and develop solutions that can be taken up and/or exploited by SMEs.

Proposals shall attempt to establish links with other projects and consortia from the Horizon Europe family (within cluster 4 or in other clusters) working on topics related to the proposal.

Note that National priorities may be applicable to specific topics (refer to Annex 5 “COUNTRY SPECIFIC ELIGIBILITY RULES”).

Actions targeted by the submitted proposals should consider contributing to building trustworthy electronics. Trusted electronics forms a foundation for a trustworthy and secure digital ecosystem, as applications need to be rooted in trustworthy components and systems. Building upon trusted and trustworthy electronics, cybersecurity techniques can be developed and relied upon to protect assets in digital systems. Electronics in this sense includes also analog functionalities to influence and sense the environment of the system e.g. by using light and photonics or other physical means. Trusted electronics can be relied upon to perform its intended functions without any unauthorized or malicious actions.

The electronic components or systems targeted by the proposed actions should meet high levels of quality and reliability, comply with known and complete specifications, and be sufficiently hardened against attacks. Technologies that are expected to increase the trustworthiness of electronics and hence the cybersecurity of embedded devices include, *inter alia*, open-source hardware, cryptographic hardware implementations combined with cryptographic software libraries, etc.

Furthermore, proposals should consider targeting key EU industrial sectors such as health, industrial automation, aerospace, or automotive.

4.1.1.4 Admissibility

Admissibility conditions are described in Annex 1 “HORIZON Europe conditions applicable to Chips JU” of the WP General Annexes.

Regarding page limits:

Chapter	**PO Stage**	**FPP Stage**
Excellence	60 pages	60 pages
Impact	60 pages	100 pages
Quality and efficiency of the Implementation	60 pages	100 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

4.1.1.5 Eligibility

Eligibility conditions: the conditions are described in Annex 1 of the WP General Annexes. The following exceptions apply:

Specific eligibility conditions:

Specific conditions	Limit
The EU contribution per project: Max Contribution per partner (% of the total EU funding) Consortium Size limit	25M 30 % 70 Participants

Proposals that do not comply to the above will be excluded.

Subject to restrictions for the protection of European communication networks (see Annex 1 of the WP General Annexes for details)

Participation is limited to legal entities established in EU Member States, Norway, Iceland, OECD and Mercosur countries (see Annex 1 of the WP General Annexes for details).

In order to guarantee the protection of the strategic interests of the Union and its Member States, entities established in an eligible country listed above, but which are directly or indirectly controlled from a non-eligible country or from a non-eligible country entity, may not participate in the action unless it can be demonstrated, by means of guarantees approved by their eligible country of establishment, in so far this is a Member State or Associated Country, that their participation to the action would not negatively impact the Union's strategic, assets, interests, autonomy, or security (see Annex 1 of the WP General Annexes for details).

For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

4.1.1.6 Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

4.1.1.7 Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

For the priority order of proposals with the same score, please refer to Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

4.1.1.8 Award criteria.

The proposals will be evaluated along the following three award criteria.

Evaluation Criteria	Project Outline Stage	Full Project Proposal Stage
Excellence	The following aspects will be taken into account, to the extent that the proposed work corresponds to the relevant description in the SRIA and complies with the scope outlined in section 4.1.1.3 on trustworthy electronics: Clarity and pertinence of the project's objectives, and the extent to which the proposed work is ambitious, and goes beyond the state of the art. Soundness of the proposed methodology.	The following aspects will be taken into account, to the extent that the proposed work corresponds to the relevant description in the SRIA and complies with the scope outlined in section 4.1.1.3 on trustworthy electronics: Clarity and pertinence of the project's objectives, and the extent to which the proposed work is ambitious, and goes beyond the state of the art. Soundness of the proposed methodology, including the underlying concepts, models, assumptions, inter-disciplinary approaches, appropriate consideration of the gender dimension in research and innovation content, and the quality of open science practices, including sharing and management of research outputs and engagement of citizens, civil

		society and end users where appropriate.
Impact	The extent to which the outputs of the project should contribute at the European and/or international level to: Credibility of the pathways to achieve the expected outcomes and impacts specified in the SRIA, and the likely scale and significance of the contributions to the project.	The extent to which the outputs of the project should contribute at the European and/or international level to: Credibility of the pathways to achieve the expected outcomes and impacts specified in the SRIA, and the likely scale and significance of the contributions to the project. Suitability and quality of the measures to maximise expected outcomes and impacts, as set out in the dissemination and exploitation plan, including communication activities.
Quality and efficiency of the implementation	The following aspects will be taken into account: Quality and effectiveness of the work plan, assessment of risks, and appropriateness of the effort assigned to work packages, and the resources overall. Extent to which the consortium as a whole brings together the necessary expertise.	The following aspects will be taken into account: Quality and effectiveness of the work plan, assessment of risks, and appropriateness of the effort assigned to work packages, and the resources overall. Capacity and role of each participant, and the extent to which the consortium brings together the necessary expertise

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

4.1.1.9 Scores

The scores will be given with a resolution of one decimal. They are valid both for PO and FPP.

Criteria	**Range**	**Weight (**)**	**Threshold (*)**
Excellence	0-5	1.0	3
Impact	0-5	1.5	3
Quality and efficiency of the implementation	0-5	0.7	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

4.1.1.10 Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to HE.

Type of beneficiary	**Maximum EU Contribution as % of the Eligible Cost according to HE (*)**
For profit organization but not an SME	20 %
SME (for profit SME)	30 %
University/Other (not for profit)	35 %

(*) beneficiaries may ask for a lower contribution.

4.1.2 Introduction: The Digital Car of the Future

The automotive industry is undergoing a transformative shift towards **software-defined vehicles (SDVs)**, driven by rapid advancements in digital technologies, electrification, and the growing demand for connected and autonomous vehicles. Unlike traditional vehicles, where functionalities are largely dictated by hardware, SDVs rely on software to define and update key features, enabling continuous improvements, customisation, and the integration of advanced technologies.

This transition represents a fundamental change in how vehicles are designed, developed, and managed. Software-defined vehicles require sophisticated software platforms, real-time over-the-air (OTA) updates, and seamless integration of artificial intelligence (AI) and machine learning (ML) technologies. These vehicles promise greater efficiency, enhanced safety, and improved sustainability by optimising performance across powertrain, infotainment, and driver-assistance systems. However, achieving these benefits demands a comprehensive redesign of the **Electrical/Electronic (E/E) architecture** within vehicles.

Traditional vehicles have historically relied on a distributed E/E architecture, where numerous electronic control units (ECUs) handle individual functionalities, such as braking, engine control, or infotainment. This fragmented approach has become increasingly impractical as vehicles evolve to incorporate more advanced features, including autonomous driving systems and connected services.

To address these challenges, the automotive industry is shifting towards **centralised E/E architectures**, which consolidate the functions of multiple ECUs into a smaller number of high-performance domain or zonal controllers. This centralisation simplifies vehicle design, reduces complexity, and enables greater computational power and data sharing across the vehicle.

Centralised E/E architectures are particularly crucial for enabling the **real-time processing of large datasets** required for autonomous driving, advanced driver-assistance systems (ADAS), and vehicle-to-everything (V2X) communication. Furthermore, they provide a scalable foundation for future innovations, allowing manufacturers to integrate new technologies with minimal disruption. Here, the RISC-V ISA and heterogeneous integration and chiplets shall be key enablers to realise novel solutions for a robust hardware platform for future automotive computing.

Moreover, from a software perspective, with the exponentially increasing complexity of in-vehicle applications, more needs to be done to leverage the use of AI, particularly generative AI, to increase productivity while maintaining all the safeguards necessary in this safety-critical domain.

For the European automotive industry, successfully navigating this transition is of critical importance. The EU has long been a leader in automotive manufacturing, but the increasing

importance of software and electronics in vehicles presents both an opportunity and a challenge. Global competition, with investments in software-driven automotive technologies accelerating, threatens Europe's position in the industry.

To this end this work programme shall include the following topics:

- RISC-V Automotive Hardware Platform
- Heterogeneous integration for high-performance automotive computing
- AI-assisted methods and tools for Software-Defined Vehicle engineering automation.

4.1.3 RISC-V Automotive Hardware Platform

Topic: HORIZON-Chips-2025-IA FT1

Type of Action	Innovation Action (IA)
Indicative EU budget	80 M€
Mode	Co-funded with the NFA Two stage Call with submission of Project Outline (PO) and of Full Proposal (FPP)
Call launch date	04 Mar 2025
Deadline PO	29 Apr 2025 at 17:00 Brussels Time
Deadline FPP Stage	17 Sep 2025 at 17:00 Brussels Time

4.1.3.1 Context

The automotive industry is currently undergoing a pivotal transformation, primarily driven by the emergence of electric, connected, autonomous, and shared (ECAS) vehicles. This shift is manifested in the conceptual framework behind automotive design, particularly in the electrical/electronic (E/E) architecture of cars. Traditionally, vehicles were designed with a multitude of independent electronic control units (ECUs) managing various functions. However, the integration of ECAS technologies necessitates a more centralised, integrated, and flexible E/E architecture. This change is essential to accommodate the advanced computing needs of autonomous driving systems, ensure seamless vehicle connectivity, support electric vehicle (EV) power management, and enable new mobility services. As a result, the automotive industry is moving towards more software-defined vehicles, where software updates can introduce new features or improvements without the need for physical alterations. Due to these trends, it is expected that the global market for automotive electronics and software will reach USD 462 billion by 2030, at a CAGR rate of 5.5%.[2]

The Digital Decade target on semiconductors i.e. '*that by 2030 the production of cutting-edge and sustainable semiconductors in Europe including processors is at least 20% of world production in value*' requires that more design activity is undertaken in Europe to create further demand to justify further investments in manufacturing in Europe. To this end, by focusing on strategic verticals, Europe can create a critical mass for demand that will act as a catalyst for the further development of a robust semiconductor industry. This focus on strategic verticals not only aligns with the EU's industrial and digital strategies, as expressed by the Chips Act

[2] Outlook on the automotive software and electronics market through 2030, McKinsey & Company

amongst other policies, but also positions the Union to become more self-sufficient and reduce its dependency on semiconductor imports.

The rising demand for high-performance in-vehicle computing is met with equally sophisticated and complex software systems. The trend towards ever-growing digitalisation and connectivity in the automotive industry leads to a widening gap between ECS complexity and productivity. As a consequence, Europe will soon face a massive talent shortage and a significant increase in ECS development costs, which calls for much more efficient, streamlined and creative engineering processes. This initiative shall be coupled with an effort to optimise software development for software defined vehicles through the use of AI.

The Chips JU has, in the last couple of years, launched several calls on RISC-V. The present call is, amongst other objectives, also meant to translate the results of those previous calls into hardware. This development is split over two calls: one that focusses on heterogenous integration process workflows and the present call that focuses on the tape out of RISC-V based processors/accelerators and their integration with other components such as memories using the heterogenous integration process flows developed in the other project.

4.1.3.2 Expected Outcomes

The overall ambition of this call is to develop in-vehicle demonstrators capable of PetaOPS computing taped-out on leading-edge processes. Proposals are expected to significantly bolster the development of a high-performance automotive RISC-V reference hardware platform, encompassing the following crucial components:

1. **High-Performance RISC-V Automotive Application Processors:** Launch of high-performance, RISC-V application processors designed for automotive applications. These processors will include advanced computer architecture techniques, multi-core configurations and support for high-bandwidth memory interfaces, catering to the complex computing demands of autonomous driving systems.
2. **AI and ML Automotive Accelerators:** Development of AI and ML accelerators with specialised ISA extensions for efficient data-intensive computations. These accelerators shall be optimised for automotive applications, supporting advanced AI models with a focus on energy efficiency and real-time processing capabilities.
3. **System Integration and Interfacing:** Establishment of a coherent system architecture integrating RISC-V cores, AI accelerators, memory and system peripherals. This includes the use of 2.5D/3D integration, the development of high-bandwidth interconnects with Quality of Service (QoS) and shared cache memories to support the high memory bandwidth required by advanced automotive applications. System 2.5/3D integration will be developed in this programme's call on heterogeneous integration for automotive.

4. **Software Tools and Libraries:** Development of a comprehensive tool-chain to support the developed RISC-V hardware. This includes compilers, binary utilities, integrated development environments (IDEs), and runtime libraries tailored for automotive applications, ensuring ease of programming and optimal performance. Hardware-software co-design is encouraged.
5. **Collaboration with the Software Defined Vehicle Initiative**: Strengthening of the open-source ecosystem through collaboration between hardware and software development, and automotive industry stakeholders. This collaborative effort will focus on alignment with other Chips Joint Undertaking projects on the Software Defined Vehicle regarding automotive standardised interfaces, middleware and APIs to facilitate seamless integration and interoperability.
6. **Benchmarking and Quality Assurance**: Implementation of benchmarking techniques to assess the performance, safety, and security of the RISC-V platforms. This will ensure compliance with automotive industry standards and regulations, paving the way for the adoption of RISC-V processors in safety-critical automotive applications.

For each of the above deliverables, achievement of key milestones demonstrating the capabilities of the RISC-V ecosystem in real automotive applications is key. These milestones will showcase the practical applications of the developed processors and accelerators in scenarios requiring high performance, real-time processing, and AI/ML computations. The culmination of the project shall include an industry-grade silicon tape-out, incorporating a competitive RISC-V application processor alongside, memory, accelerators and any other relevant IP taking advantage of advanced packaging techniques. This shall be accompanied by a mature toolset.

Targeted TRL at the end of project is between 7 and 8.

4.1.3.3 Scope

The scope of the call is to address Europe's technological sovereignty in automotive processors and accelerators. Proposals submitted to this call should address the following elements:

- high-performance RISC-V automotive application processors;
- artificial intelligence (AI) and machine learning (ML) automotive accelerators;

The developments under this initiative, while purely pre-competitive in nature, should have a clear perspective towards eventual commercialisation by European industry. The results shall include **tangible silicon demonstrators** that can be deployed in an operational environment as qualified devices. Proposals should clearly target the requirements of the European automotive industry. Where appropriate, proposals submitted in response to this call should consider the potential application of the aforementioned elements in other industry verticals.

This call is precompetitive and aims to develop a common European platform for automotive processors and accelerators. A proposal should include processors/accelerators taped-out using leading-edge technologies and multiple tape-outs.

Consortia submitting applications to this call should be inclusive, incorporating the relevant stakeholders across the microelectronics and automotive value-chain such as Integrated Device Manufacturers (IDMs), automotive Original Equipment Manufacturers (OEMs) and Tier 1 suppliers and if relevant Research and Technology Organisations (RTOs). Furthermore, consortia should include credible start-ups and SMEs that have the potential of exploiting the results of the projects under this call and develop into European champions. Nevertheless, the consortia should be focussed on the objectives and each partner should have a well-defined essential role towards the achievement of the objectives. The proposal should describe the role and why it is essential for each partner to participate.

The proposal should present and maintain a comprehensive, medium-term implementation roadmap. This roadmap must outline a stringent yet achievable timeline and set ambitious milestones for the necessary actions to establish a processor ecosystem targeted towards the automotive industry. The roadmap should also take into consideration other related EU and Member State funded projects. This roadmap shall convincingly indicate how the results of this project shall **reach global-state-of-the-art** by the time the project concludes and **eventually be adopted by automotive OEMs upon industrialisation**.

Proposals should present an action plan that addresses the different outcomes elaborated above with significant milestones clearly indicated for each outcome. To this end, the applying consortium must define a robust governance structure to ensure a well-managed, coordinated and coherent action across all streams and objectives of this call.

The proposals submitted to this call should include an extensive description on how IP generated in the initiative is handled for the benefit of the EU, with due consideration to IP management, protection and exploitation.

Additionally, proposals should provide an overview of current technology trends in the sector and explain how the proposed work under this action will contribute to European leadership vis-a-vis global competition.

This should be complemented by the definition of clear KPIs that are benchmarked against non-EU competitors for the project. Proposals should include activities to liaise with the projects selected in the two other focus topics. In particular the selected proposals for the present call and the call on heterogenous integration will have to align their activities, roadmaps, milestones, transfer of results and IP, etc. in order for the present call to be able to build the required demonstrators.

Collaboration with Chips JU projects such as RIGOLETTO, TRISTAN and ISOLDE, should be sought after.

Efforts shall be made to synergise with the EuroHPC FPA on RISC-V for High-Performance Computing.[3] Where relevant, proposals should consider synergies with the pilot lines and design platforms developed within the framework of the Chips Act's Chips for Europe Initiative.[4]

4.1.3.4 Admissibility

Admissibility conditions are described in Annex 1 "General HORIZON Europe conditions" of the WP General Annexes.
Regarding page limits:

Chapter	PO Stage	FPP Stage
Excellence	60 pages	60 pages
Impact	60 pages	100 pages
Quality and efficiency of the Implementation	60 pages	100 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

4.1.3.5 Eligibility

Eligibility conditions are described in Annex 1 of the WP General Annexes. The following exceptions apply:

Specific eligibility conditions:

[3] Framework Partnership Agreement (FPA) for developing a large-scale European initiative for High Performance Computing (HPC) ecosystem based on RISC-V - EuroHPC JU (europa.eu)
[4] Chips for Europe Initiative · Chips Ju (europa.eu)

Subject to restrictions for the protection of European communication networks (see Annex 1 of the WP General Annexes for details)

Participation is limited to legal entities established in EU Member States, Norway, Iceland, Associated Countries, OECD and Mercosur countries (see Annex 1 of the WP General Annexes for details).

In order to guarantee the protection of the strategic interests of the Union and its Member States, entities established in an eligible country listed above, but which are directly or indirectly controlled from a non-eligible country or from a non-eligible country entity, may not participate in the action unless it can be demonstrated, by means of guarantees approved by their eligible country of establishment, in so far this is a Member State or Associated Country, that their participation to the action would not negatively impact the Union's strategic, assets, interests, autonomy, or security (see Annex 1 of the WP General Annexes for details).

Specific conditions	Limit
Size limit	35 Participants
Recommended SME's share of participants	1/3 of participants

For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

4.1.3.6 Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

4.1.3.7 Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

4.1.3.8 Award criteria.

Award criteria are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

4.1.3.9 Scores

The scores will be given with a resolution of one decimal.

Criteria	Range	Weight (**)	Threshold (*)
Excellence	0-5	1.0	3
Impact	0-5	1.5	3
Quality and efficiency of the implementation	0-5	0.7	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

4.1.3.10 Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to HE.

Type of beneficiary	Maximum EU Contribution as % of the Eligible Cost according to HE (*)
For profit organization but not an SME	25 %
SME (for profit SME)	35 %

University/Other (not for profit)	35 %

(*) beneficiaries may ask for a lower contribution.

4.1.4 AI-assisted Methods and Tools for Software-Defined Vehicle Engineering Automation

Topic: HORIZON-Chips-2025-IA FT2

Type of Action	Innovation Action (IA)
Indicative EU budget	20 M€
Mode	Co-funded with the NFA Two stage Call with submission of Project Outline (PO) and of Full Proposal (FPP)
Call launch date	04 Mar 2025
Deadline PO	29 Apr 2025 at 17:00 Brussels Time
Deadline FPP Stage	17 Sep 2025 at 17:00 Brussels Time
Technology Readiness Level	The activities must have their centre of gravity at TRL 6-7 at the end of the project.

4.1.4.1 Context

This Focus Topic is part of the European Digital Vehicle[5] initiative.

Modern ECS are a highly complex combination of hardware and software components that exhibit intricate configurations, dependability constraints and interoperability needs. The trend toward ever-growing digitalization and connectivity in a knowledge-intensive society leads to a widening gap between ECS complexity and productivity. As a consequence, Europe is already facing a massive talent shortage and a significant increase in ECS development costs, which calls for much more efficient, streamlined and creative engineering processes.

While engineering automation frameworks have already been deployed upwards of hundreds of software tools used by large teams of engineers, there are a number of barriers to their massive adoption in the ECS industry, and in particular in the high-assurance ECS market. The emergence of Artificial Intelligence (AI) opens new possibilities for overcoming these barriers, from substantially scaling the ability of handling complexity, to improving the capability to manage multi-risk assurance problems and providing much better guidance and experience to

[5] Previously called 'Vehicle of the Future' initiative. For more information, consult https://digital-strategy.ec.europa.eu/en/policies/vehicle-future-initiative

engineers. ***AI offers a paradigm shift to focus the scarce human engineering resources in more creative and innovative tasks***.

The vision behind this topic is to ***massively accelerate ECS engineering efficiency through software engineering automation based on an expanded use of AI-assisted methods and tools***, by building upon a cohesive collaboration between humans (with their ability to innovate and create intuitive solutions) and AI (with its ability to propose solutions exploring huge search spaces and recognizing statistical patterns from large data). This focus topic shall lead to a stronger competitive position of Europe in ECS engineering worldwide and stimulate the uptake of AI-powered methods and tools for improved engineering efficiency, by still helping with better understanding and broader acceptance of such technologies.

This trend is particularly strong in the automotive industry, where the complexity of software and electronic hardware is surging due to the growing automation, electrification and demand for advanced in-vehicle experience. In the era of software-defined vehicles (SDVs), the industry has to shift to different ways to build software and electronic hardware to gain agility and development speed. Currently, automotive suppliers and manufacturers spend a lot of resources and time to adapt ECS systems to different automotive platforms, which is reducing their productivity and competitiveness. Standardisation and collaborative ecosystems based on open platforms, architectures and processes are essential to allow multiple different companies to work together seamlessly, facilitating the integration of systems and components from multiple vendors. Being safety-critical systems, vehicles need to fulfil stringent safety and security standards and legislation. This creates specific issues for all stages of the ECS development processes, notably regarding verification, validation and preparation for certification.

This focus topic is part of the Software-defined Vehicle Focus Area of the European Digital Vehicle Initiative. Selected actions will be implemented as '**linked actions**', i.e. they are linked with other actions selected under '*SDV Vehicle of the Future'* topics in past calls, this call and future calls, e.g. HORIZON-KDT-JU-2023-2-RIA ***Focus-Topic 2 on Hardware abstraction layer for a European Vehicle Operating System*** and HORIZON-Chips-2024-1-IA Focus-Topic 3 **on Software-define vehicle middleware and API framework for the vehicle of the future**. The notion of "linked actions" may as well be extended to other EU-supported actions, e.g. HORIZON-Chips-2024-1-IA Focus-Topic 3 on **High Performance RISC-V Automotive Processors supporting SDV,** or actions under the CCAM and 2ZERO partnerships. A **collaboration agreement** with other selected projects and future projects should be established, that sets out requirements for **IP sharing**, a **common governance model**, and **conformity** with specifications set by suitable industry bodies. Respective options under Article 3 and Article 7 of the Model Grant Agreement will be used to this end.

4.1.4.2 Expected Outcomes

The project is expected to contribute to the following outcomes:

- ***Advanced AI-assisted methods and tools***, including generative AI, for the automation of software engineering tasks, from enhancing human efficiency and optimizing resource utilization to enabling complex data/problems analysis/interpretation and supporting intelligent decision-making. Such engineering tasks often involve multiple domains (e.g., modelling, control, data management, communication, mechatronics, etc.) and stakeholders, with the burden of daunting legacy integration, refactoring (e.g., to re-design and replace obsolete technology), and the compliance with specific standards, regulations and certifications.
- ***Open and extensible AI-assisted integrated platform,*** based on methodologies including AI-support, AI-based tools and toolchains, following a well-defined engineering process, including the integration with legacy tools. The platform shall provide flexible usage in small and large multi-domain and multi-stakeholder engineering teams, impacting existing and upcoming ECS engineering automation tools and their usage.
- ***Showcasing and evaluation*** for software-defined vehicles of efficiency enhancements in terms of cost and time for complex data/knowledge management, resource optimization, energy consumption, interoperability, product/process quality/trustworthiness, learning curve and usability, over the whole lifecycle, from design, through deployment, operations, and maintenance, to the product end-of-life and recycling, and its evolution.
- ***Best practices and small proof-of-concept studies for other sectors***, e.g. medical/pharmaceutical and/or digital industry.

4.1.4.3 Scope

Proposals should particularly address the following aspects:

- The targeted ECS-based products to be engineered by the AI-assisted engineering solutions shall focus on embedded and cyber-physical systems and system of systems that operate in (safety, security and reliability) high-assurance, regulated domains. The common aspects between these ECS-based products are: (i) a lifecycle requiring HW/SW/multi-physical co-engineering, and (ii) their highly complex and potentially distributed nature, e.g. impacting on the necessity to holistically handle the explosion in the number of design parameters and constraints as well as the components and their combination.
- Adoption of generative AI in the software engineering process, to automate repetitive tasks, creating software models and architectures (model-driven development and design tools), generating code snippets (code generators, automated refactoring and code optimization, assisted code completion), test and debugging (automated testing and test case generation, automated debugging and bug detection), documentation (NLP for documentation editing

and requirements elicitation) and providing support for software lifecycle (AI-driven DevOps and deployment/commissioning optimization).

- AI-based engineering solutions should be largely domain independent but shall be adopted and showcased primarily in the software layers of the European Digital Vehicle technology stack (SDV). Showcasing and demonstration shall cover test, validation and evaluation in the domain of the SDV and shall also identify best practices for other vertical domains (e.g. medical/pharmaceutical and/or digital industry).
- AI shall ensure assistance in two main stages of the engineering process, potentially extending to the entire lifecycle of ECS-based products: (i) design, development, customisation, and maintenance, and (ii) verification and validation (including simulation, co-simulation, test, etc.), and certification. AI-assisted methods, tools and integrated platform aim at alleviating engineers' work in routine activities, supporting them in complex tasks, facilitating/ensuring the consolidation and growth of their expertise, and supporting multidisciplinary multistakeholder team-work, e.g.:
    - requirement engineering and their refinement,
    - embedded and cyber-physical systems modelling, simulation and co-simulation,
    - (real or near real-time) data management, e.g., data cleaning, analysis, enrichment, classification, labelling,
    - visual interpretation of high-dimensional data,
    - code generation, debugging and refactoring (e.g., using generative AI),
    - search of the design/validation/verification spaces for multi-criteria optimization,
    - generation of test datasets along continuous testing,
    - best-design practice guidance,
    - professional training,
    - interoperability along the continuous engineering life cycle,
    - seamless interaction with/between designers and other stakeholders.
- The dimension of human-AI integration in the engineering process shall improve efficiency and productivity, facilitate collaborative discovery, adaptivity, and continuous co-learning from perspectives that are not only technical but also human centred such as new creation fashions, higher comfort, stress and effort reduction, higher satisfaction, ethics compliance, etc. Cooperation between multidisciplinary partners with background in AI/automation, tooling development and the specific system to be engineered, is required to succeed.
- The proposed AI-assisted methods and tools must handle multi-risk problems in a way that are digestible by the engineers in the domain. The evolutionary nature of advanced ECS products (likely containing AI) could potentially generate safety, security, privacy, and other trustworthiness risks that are a big concern of regulatory, certification and/or quality assurance bodies. The involvement of regulators, certification and standardisation bodies is encouraged to understand regulatory limits of using such AI-assisted engineering solutions.

- The architecture of the proposed engineering solutions and the targeted open and extensible AI-assisted integrated platform shall support service-oriented business models and model-based engineering approaches to avoid fragmentation and unnecessary overlapping, facilitate tools and toolchains interoperability and integration (including legacy tools and toolchains), and ensure the platform evolution. This platform shall include guidance for selecting and using the tools, continuous monitoring/assessment of the maturity and new features of the tools, proper governance targeting sustainability, and support for education and training. Particular focus is expected on the identification, inception and proposal of de facto or de jure standards covering procedures, models, taxonomies and APIs for AI-based engineering processes.
- While the developments at the end of the project have their centre of gravity at TRL 5-6, the project can also target lower TRLs for some specific activities if they are well justified in terms of concrete innovation opportunities.

Relevant aspects:

- Involve in the project a significant and - at each level - representative number of actors across the European automotive value chain from OEMs and Tier 1 suppliers to general and sector-specific engineering tool providers – large and small.
- Ensure a strong participation of SMEs and start-ups in solution developments, paying attention to developing solutions that can be taken up and/or exploited with fast and simple access to standardized and business-friendly open-source solutions.
- Include leading universities and research and technology organisations bringing the newest advances in SW engineering tolls as well as AI and generative AI.
- Allocate tasks to cohesion activities with the project(s) selected under the call HORIZON-KDT-JU-2023-2-RIA Focus-Topic 2 on Hardware abstraction layer for a European Vehicle Operating System, HORIZON-Chips-2024-1-IA Focus-Topic 3 on Software-define vehicle middleware and API framework for the vehicle of the future, and HORIZON-Chips-2024-1-IA Focus-Topic 3 on High Performance RISC-V Automotive Processors supporting SDV.

4.1.4.4 Admissibility

Admissibility conditions are described Annex 1 “HORIZON Europe conditions applicable to Chips JU” of the WP General Annexes.

Regarding page limits:

Chapter	PO Stage	FPP Stage

Excellence	60 pages	60 pages
Impact	60 pages	100 pages
Quality and efficiency of the Implementation	60 pages	100 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

4.1.4.5 Eligibility

Eligibility conditions are described in Annex 1 of the WP General Annexes. The following exceptions apply:

Specific eligibility conditions:

Subject to restrictions for the protection of European communication networks (see Annex 1 of the WP General Annexes for details)

Participation is limited to legal entities established in EU Member States, Norway, Iceland, Associated Countries, OECD and Mercosur countries (see Annex 1 of the WP General Annexes for details).

In order to guarantee the protection of the strategic interests of the Union and its Member States, entities established in an eligible country listed above, but which are directly or indirectly controlled from a non-eligible country or from a non-eligible country entity, may not participate in the action unless it can be demonstrated, by means of guarantees approved by their eligible country of establishment, in so far this is a Member State or Associated Country, that their participation to the action would not negatively impact the Union's strategic, assets, interests, autonomy, or security (see Annex 1 of the WP General Annexes for details).

Specific conditions	Limit
Size limit	40 Participants

For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

4.1.4.6 Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

4.1.4.7 Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

For the priority order of proposals with the same score, please refer to Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

4.1.4.8 Award criteria.

Award criteria are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

4.1.4.9 Scores

The scores will be given with a resolution of one decimal. The score table is valid for PO and FPP.

Criteria	**Range**	**Weight (**)**	**Threshold (*)**
Excellence	0-5	1.0	3
Impact	0-5	1.5	3

Quality and efficiency of the implementation	0-5	0.7	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

4.1.4.10 Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to HE.

Type of beneficiary	**Maximum EU Contribution as % of the Eligible Cost according to HE (*)**
For profit organization but not an SME)	25 %
SME (for profit SME)	35 %
University/Other (not for profit)	35 %

(*) beneficiaries may ask for a lower contribution.

4.2 Call on Heterogeneous integration for high-performance automotive computing.

Topic: HORIZON-Chips-2025-IA HIA

Type of Action	Innovation Action (IA)
Indicative EU budget	20 M€
Mode	Co-funded with the NFA One stage Call
Call launch date	04 Mar 2025
Deadline	29 Apr 2025 at 17:00 Brussels Time

4.2.1.1 Context

Moore's law is reaching its practical limits while at the same time computing demands — including those within the vehicle — are increasing. As complexity rises with technology node miniaturisation, design and fabrication costs are increasing exponentially from one leading edge node to the next.

Considering the volumes of the automotive industry and the computing demands of the vehicle of the future, requiring more advanced nodes, monolithic SoCs at the leading edge incorporating all of the IP blocks necessary are untenable.

Heterogeneous integration, particularly through 2.5D and 3D technologies, presents a promising solution for meeting the growing demands of a more autonomous and connected future. Chiplet-based designs enable the integration of dies fabricated at different process nodes, offering a cost-effective approach due to improved yield rates, and faster time-to-market.

Additionally, chiplet architectures promote innovation and differentiation through their modular design. By allowing the mix-and-match of various functional blocks, these architectures provide greater flexibility, making it easier for customers to customise and upgrade computing components, driving scalability and adaptability in modern systems.

The Chips JU has in the last couple of years supported several projects on heterogenous integration. The present call is, amongst other objectives, also meant to translate the results of those previous calls into process workflows (TRL 7-8). Implementation of the developed

workflows will be integrated in the call on RISC-V hardware platform. This will require a close collaboration between the two consortia that will be enforced when preparing the grants.

4.2.1.2 Expected outcomes.

Proposals are expected to encompass at least the following elements:

1. **Automotive chiplet system framework**: Develop and implement the architectural and design specifications for an automotive chiplet-based computing platform, taking into consideration any relevant standards and industry wide collaborations in this field.
2. **Adaptation of relevant IP**: Where necessary, adapt pertinent intellectual property (IP) to support seamless chiplet integration within the automotive context.
3. **Automotive base die development**: Development of an *automotive base die* for the orchestration of in-package computing with adequate process workflows.
4. **System Integration and Packaging**: integrate the system and develop the package taking into consideration automotive requirements.

Complementarity with the RISC-V Automotive Hardware Platform topic is expected. For the purposes of intermediate physical demonstrators, non-RISC-V based IP may be considered for in-package integration. Collaboration with the Chips for Europe Initiative pilot lines is encouraged. Nevertheless, the final deliverable for this project should include components developed under the RISC-V Automotive Hardware Platform call - particularly the application processor and AI accelerators - integrated with other IP via the chiplet platform developed under this call.

4.2.1.3 Scope

Proposals submitted to this call should address heterogeneous integration and interfacing components with special emphasis on 2.5D integration through chiplets.

The developments under this initiative, while purely pre-competitive in nature, should have a clear perspective towards eventual commercialisation by European industry. The results shall include **tangible silicon demonstrators** that can be deployed in an operational environment as qualified devices. Proposals submitted to this call should clearly target the requirements of the European automotive industry. Where appropriate, proposals submitted in response to this call should consider the potential application of the aforementioned elements in other industry verticals.

Consortia submitting applications to this call should be inclusive, incorporating the relevant stakeholders across the microelectronics and automotive value-chain such as Integrated Device Manufacturers (IDMs), automotive Original Equipment Manufacturers (OEMs) and Tier 1 suppliers and if relevant Research and Technology Organisations (RTOs). Furthermore, consortia should include credible start-ups and SMEs that have the potential of exploiting the

results of the projects under this call and develop into European champions. Nevertheless, the consortia should be focussed on the objectives and each partner should have a well-defined essential role towards the achievement of the objectives. The proposal must describe the role and why it is essential for each partner. A consortium with around 15 participants (or less) should be able to cover all the required tasks. The proposal should present and maintain a comprehensive, medium-term implementation roadmap. This roadmap must outline a stringent yet achievable timeline and set ambitious milestones for the necessary actions to establish a processor ecosystem targeted towards the automotive industry. The roadmap should also take into consideration other related EU and Member State funded projects. This roadmap shall convincingly indicate how the results of this project shall **reach global-state-of-the-art** by the time the project concludes and eventually be adopted by automotive OEMs upon industrialisation.

Proposals should present an action plan that addresses the different outcomes elaborated below with significant milestones clearly indicated for each outcome. To this end, the applying consortium must define a robust governance structure to ensure a well-managed, coordinated and coherent action across all streams and objectives of this call.

The selected proposals for the present call and the call on the RISC-V Automotive Hardware Platform must align their activities, roadmaps, milestones, transfer of results and IP, etc. to realise the required demonstrators.

Collaboration with other Chips JU projects in this domain should be sought after.

4.2.1.4 Admissibility

Admissibility conditions are described in Annex 1 “HORIZON Europe conditions applicable to Chips JU” of the WP General Annexes.

Regarding page limits:

Chapter	**PO Stage**	**FPP Stage**
Excellence	60 pages	60 pages
Impact	60 pages	100 pages
Quality and efficiency of the Implementation	60 pages	100 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

4.2.1.5 Eligibility

Eligibility conditions are described in Annex 1 of the WP General Annexes.

The following exceptions apply:

Specific conditions	Limit
Size limit	35 Participants
Recommended SME's share of participants	1/3 of participants

Subject to restrictions for the protection of European communication networks (see Annex 1 of the WP General Annexes for details)

Participation is limited to legal entities established in EU Member States, Norway, Iceland, Associated Countries, OECD and Mercosur countries (see Annex 1 of the WP General Annexes for details).

In order to guarantee the protection of the strategic interests of the Union and its Member States, entities established in an eligible country listed above, but which are directly or indirectly controlled from a non-eligible country or from a non-eligible country entity, may not participate in the action unless it can be demonstrated, by means of guarantees approved by their eligible country of establishment, in so far this is a Member State or Associated Country, that their participation to the action would not negatively impact the Union's strategic, assets, interests, autonomy, or security (see Annex 1 of the WP General Annexes for details).
For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

4.2.1.6 Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

4.2.1.7 Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

For the priority order of proposals with the same score, please refer to Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

4.2.1.8 Award criteria.

Award criteria are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

4.2.1.9 Scores

The scores will be given with a resolution of one decimal.

Criteria	**Range**	**Weight (**)**	**Threshold (*)**
Excellence	0-5	1.0	3
Impact	0-5	1.5	3
Quality and efficiency of the implementation	0-5	0.7	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

4.2.1.10 Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to HE.

Type of beneficiary	**Maximum EU Contribution as % of the Eligible Cost according to HE (*)**
For profit organization but not an SME	25 %
SME (for profit SME)	35 %
University/Other (not for profit)	35 %

(*) beneficiaries may ask for a lower contribution.

4.3 ECS GLOBAL RIA

4.3.1 Global RIA

Topic: HORIZON-Chips-2025-RIA

Type of Action	Research and Innovation Action (IA)
Indicative EU budget	40 M€
Mode	Co-funded with the NFA Two stage Call with submission of Project Outline (PO) and of Full Proposal (FPP)
Call launch date	04 Mar 2025
Deadline PO	29 Apr 2025 at 17:00 Brussels Time
Deadline FPP Stage	17 Sep 2025 at 17:00 Brussels Time

4.3.1.1 Context

This topic is the RIA-part of the bottom-up programming. The topic will be open to the major challenges addressed in the current version of the Chips JU Strategic Research and Innovation Agenda, excluding the topics addressed in the focus topics of all the HE Chips JU calls in 2025 (ECS and Chips for Europe calls).

Aspects of ECS value chain integration are important for the Chips JU programme and the whole European ECS sector, across applications and across capabilities, as well as cutting across disciplines, supporting platform building, interoperability, establishing open standards. The participation of SMEs in the developments allowing them to play effective roles while working on solutions that can be taken exploited by SMEs is important in view of the SBA.

4.3.1.2 Expected outcomes.

A Chips JU Research and Innovation Action (RIA) primarily consists of activities aiming to establish new knowledge and/or to explore the feasibility of a new or improved technology, product, process, service, method, tool or solution. For this purpose, they may include applied research, technology development and/or method/tool and integration, testing and validation on a small-scale prototype in a laboratory or simulated environment. The activities have their centre of gravity at TRL 3-4.

A RIA proposal is characterised by:

- Execution by a consortium that may consist of SMEs, large enterprises, universities, institutes, public organizations;
- Developing innovative technologies and/or using them in innovative ways;
- Targeting demonstration of the innovative approach in a relevant product, service or capability, clearly addressing the applications relevant for societal challenges;
- Demonstrating value and potential in a realistic lab environment reproducing the targeted application;
- Having a deployment plan showing the valorisation for the Chips JU ecosystem and the contribution to the Chips JU goals and objectives.

In order to maximize effective implementation of the Chips JU top-level objectives, the list of RIA proposals to be retained for public funding shall constitute a balanced portfolio of projects developing innovative technologies (as defined in the SRIA in the functional technology layers and cross-sectional technologies sections) and applying them in different domains (as defined in the SRIA in key application areas section). The domains represent the demand side of technologies, and the development of new technologies represents the supply side of technologies.

4.3.1.3 Scope

This topic is the RIA part of the bottom-up programming. The topic will be open to the following major challenges as defined in the SRIA:

Topics and Major Challenges		Open/Closed
1.1 - Process technology, equipment, materials and manufacturing		
	Major Challenge 1: Advanced computing, in-memory, neuromorphic, photonic, and quantum computing concepts	Open
	Major Challenge 2: Novel sensor, actuation and other devices that enable advanced functionality	Open
	Major Challenge 3: Advanced integration solutions	Open
	Major Challenge 4: Advanced wafer fab equipment and manufacturing solutions	Open
	Major Challenge 5: Advanced packaging, assembly & test equipment solutions	

	Major Challenge 6: Sustainable semiconductor manufacturing	
1.2 - Components, modules and systems integration		
	Major Challenge 1: Functionality	Open
	Major Challenge 2: Advanced Integration solutions	Open
	Major Challenge 3: Heterogenous integration	Open
	Major Challenge 4: Sustainability	
1.3 - Embedded software and beyond		
	Major Challenge 1: Efficient engineering of embedded software	Open
	Major Challenge 2: Continuous integration and deployment	Open
	Major Challenge 3: Lifecycle management	Open
	Major Challenge 4: Embedding data analytics and Artificial Intelligence	Open
	Major Challenge 5: Support for Sustainability by embedded software	Open
	Major Challenge 6: Software reliability and trust	Open
	Major Challenge 7: Hardware virtualization for efficient SW engineering	Open
1.4 - System of Systems		
	Major Challenge 1: Open SoS architecture and infrastructure	Open
	Major challenge 2: SoS interoperability	Open
	Major Challenge 3: Evolvability of SoS composed of embedded and cyber-physical systems	Open
	Major Challenge 4: SoS integration along the life cycle	Open
	Major Challenge 6: SoS monitoring and management	Open
2.1 - Edge Computing and Embedded Artificial Intelligence		
	Major Challenge 1: Increasing energy efficiency	Open
	Major Challenge 2: Managing the increasing complexity of systems	Open
	Major Challenge 3: Supporting the increasing lifespan of devices and systems	Open
	Major Challenge 4: Ensuring European sustainability	Open
2.2 – Connectivity		

	Major Challenge 1: Strengthening the EU connectivity technology portfolio to maintain leadership, secure sovereignty and offer an independent supply chain	Open
	Major Challenge 2: Investigate innovative connectivity technology (new spectrum or medium) and new approaches to improving existing connectivity technology to maintain the EU's long-term leadership	Open
	Major Challenge 3: Autonomous interoperability translation for communication protocol, data encoding, compression, security and information semantics	Open
	Major Challenge 4: Architectures and reference implementations of interoperable, secure, scalable, smart and evolvable IoT and SoS connectivity from edge to cloud	Open
	Major Challenge 5: Network virtualisation enabling run-time and evolvable integration, deployment and management of edge to cloud network architectures	Open
2.3 - Architecture and design: methods and tools		
	Major Challenge 1: Enabling cost- and effort-efficient Design and Validation Frameworks for High Quality ECS. The ever-increasing functionality of ECS, usage and integration of new technologies to enable these functions and the high demands for validation and testing to ensure their quality drive the need for efficient, framework- and tool-supported design and validation processes and frameworks.	Open
	Major Challenge 2: Enabling Sustainable Design for Sustainability. Methods and tools to support the design and validation of sustainable ECS as well as supporting a sustainable design and validation process.	Open
	Major Challenge 3: Managing complexity. This challenge deals with methods to handle the ever-increasing complexity of ECS-based systems.	Open
	Major Challenge 4: Managing diversity. Handling diversity in all aspects of developing ECS-based systems is the key objective of this challenge.	Open
2.4 - Quality, reliability, safety and cybersecurity		
	Major Challenge 1: Ensuring HW quality and reliability	Open
	Major Challenge 2: Ensuring dependability in connected software	Open
	Major Challenge 3: Ensuring cyber-security and privacy	Open
	Major Challenge 4: Ensuring of safety and resilience	Open

	Major Challenge 5: Human systems integration	Open
3.1 – Mobility		
	Major Challenge 1: SDV hardware platforms: modular, scalable, flexible, safe & secure	**Closed**
	Major Challenge 2: SW platforms for SDV of the future: modular, scalable, re-usable, flexible, safe & secure, supporting edge2cloud applications	Open
	Major Challenge 3: Green deal: enable climate and energy optimal mobility	Open
	Major Challenge 4: Digitalisation: affordable and safe automated and connected mobility for passengers and freight	Open
	Major Challenge 5: Edge2cloud mobility applications: added end-user value in mobility	Open
	Major Challenge 6: AI enabled engineering tool chain: agile collaborative SDV SW development and SDV as well as ADAS/AD validation	**Closed**
3.2 – Energy		
	Major Challenge 1: Smart & Efficient - Managing Energy Generation, Conversion, and Storage Systems	Open
	Major Challenge 2: Energy Management from On-Site to Distribution Systems	Open
	Major Challenge 3: Future Transmission Grids	Open
	Major Challenge 4: Achieving Clean, Efficient & Resilient Urban/ Regional Energy Supply	Open
	Major Challenge 5: Cross-Sectional Tasks for Energy System Monitoring & Control	Open
3.3 - Digital Industry		
	Major challenge 1: Responsive and smart production	Open
	Major challenge 2: Sustainable production	Open
	Major challenge 3: Artificial Intelligence in digital industry	Open
	Major challenge 4: Industrial service business, lifecycles, remote operations and teleoperation	Open

	Major challenge 5: Digital twins, mixed or augmented reality, telepresence	Open
	Major challenge 6: Autonomous systems, collaborative robotics	Open
3.4 - Health and wellbeing		
	Major Challenge 1: Enable digital health platforms based upon P4 healthcare	Open
	Major Challenge 2: Enable the shift to value-based healthcare, enhancing access to 4P's game-changing technologies	Open
	Major Challenge 3: Support the development of the home as the central location of the patient, building a more integrated care delivery system	Open
	Major Challenge 4: Enhance access to personalised and participative treatment for chronic and lifestyle-related diseases	Open
	Major Challenge 5: Ensure more healthy life years for an ageing population	Open
3.5 - Agrifood and natural resources		
	Major Challenge 1: Food security	Open
	Major Challenge 2: Food safety	Open
	Major Challenge 3: Environmental protection and sustainable production	Open
	Major Challenge 4: Water resource management	Open
	Major Challenge 5: Biodiversity restoration for ecosystems resilience, conservation and preservation	Open
3.6 - Digital Society		
	Major Challenge 1: Facilitate individual self-fulfilment	Open
	Major Challenge 2: Facilitate empowerment and resilience	Open
	Major Challenge 3: Facilitate inclusion and collective safety	Open
	Major Challenge 4: Facilitate supportive infrastructure and a sustainable environment	Open

Detailed descriptions of all major challenges can be found in the SRIA.

Aspects of ECS value chain integration are important for the Chips JU programme and the whole European ECS sector, across applications and across capabilities. Consortia are encouraged to submit proposals that take this aspect into account.

Proposals that cut across disciplines, support platform building, interoperability, establishment of open standards are particularly encouraged; even outside the regular ECS sector.

Proposals shall encourage SMEs to participate in the developments, in particular paying attention to the needs of SMEs, involve SMEs in project execution, and develop solutions that can be taken up and/or exploited by SMEs.

Proposals shall attempt to establish links with other projects and consortia from the Horizon Europe family (within cluster 4 or in other clusters) working on topics related to the proposal.

Note that National priorities may be applicable to specific topics (refer to Annex 5 "COUNTRY SPECIFIC ELIGIBILITY RULES").

4.3.1.4 Admissibility

Admissibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Regarding page limits:

Chapter	**PO Stage**	**FPP Stage**
Excellence	60 pages	60 pages
Impact	60 pages	100 pages
Quality and efficiency of the Implementation	60 pages	100 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

4.3.1.5 Eligibility

Eligibility conditions are described in Annex 1 of the WP General Annexes. The following exceptions apply:

Specific eligibility conditions:

Subject to restrictions for the protection of European communication networks (see Annex 1 of the WP General Annexes for details).

Participation is limited to legal entities established in EU Member States, Norway, Iceland, Associated Countries, OECD and Mercosur countries (see Annex 1 of the WP General Annexes for details).

In order to guarantee the protection of the strategic interests of the Union and its Member States, entities established in an eligible country listed above, but which are directly or indirectly controlled from a non-eligible country or from a non-eligible country entity, may not participate in the action unless it can be demonstrated, by means of guarantees approved by their eligible country of establishment, in so far this is a Member State or Associated Country, that their participation to the action would not negatively impact the Union's strategic, assets, interests, autonomy, or security (see Annex 1 of the WP General Annexes for details).

The EU contribution per project is capped at:	• 12M
Max Contribution per partner (% of the total EU funding)	30 %
Consortium Size limit	50 Participants

Proposals that do not comply to the above will be excluded.

For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

4.3.1.6 Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

4.3.1.7 Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

For the priority order of proposals with the same score, please refer to Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

4.3.1.8 Award criteria.

The proposals will be evaluated along the following three evaluation criteria.

Evaluation Criteria	Project Outline Stage	Full Project Proposal Stage
Excellence	The following aspects will be taken into account, to the extent that the proposed work corresponds to the relevant description in the SRIA: Clarity and pertinence of the project's objectives, and the extent to which the proposed work is ambitious, and goes beyond the state of the art. Soundness of the proposed methodology.	The following aspects will be taken into account, to the extent that the proposed work corresponds to the relevant description in the SRIA: Clarity and pertinence of the project's objectives, and the extent to which the proposed work is ambitious, and goes beyond the state of the art. Soundness of the proposed methodology, including the underlying concepts, models, assumptions, inter-disciplinary approaches, appropriate consideration of the gender dimension in research and innovation content, and the quality of open science practices, including sharing and management of research outputs and engagement of citizens, civil society and end users where appropriate.

Impact	The extent to which the outputs of the project should contribute at the European and/or international level to: Credibility of the pathways to achieve the expected outcomes and impacts specified in the SRIA, and the likely scale and significance of the contributions to the project.	The extent to which the outputs of the project should contribute at the European and/or international level to: Credibility of the pathways to achieve the expected outcomes and impacts specified in the SRIA, and the likely scale and significance of the contributions to the project. Suitability and quality of the measures to maximise expected outcomes and impacts, as set out in the dissemination and exploitation plan, including communication activities.
Quality and efficiency of the implementation	The following aspects will be taken into account: Quality and effectiveness of the work plan, assessment of risks, and appropriateness of the effort assigned to work packages, and the resources overall. Extent to which the consortium as a whole brings together the necessary expertise.	The following aspects will be taken into account: Quality and effectiveness of the work plan, assessment of risks, and appropriateness of the effort assigned to work packages, and the resources overall. Capacity and role of each participant, and the extent to which the consortium brings together the necessary expertise.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

4.3.1.9 Scores

The scores will be given with a resolution of one decimal. The score table is valid for PO and FPP.

Criteria	Range	Weight (**)	Threshold (*)
Excellence	0-5	1.0	3
Impact	0-5	1.5	3
Quality and efficiency of the implementation	0-5	0.7	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

4.3.1.10 Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to HE.

Type of beneficiary	Maximum EU Contribution as % of the Eligible Cost according to HE (*)
For profit organization but not an SME	25 %
SME (for profit SME)	35 %
University/Other (not for profit)	35 %

(*) beneficiaries may ask for a lower contribution.

4.4 International Cooperation

4.4.1 Boosting R&I cooperation between EU and Japan on semiconductors

Topic: HORIZON-Chips-2025-CSA

Type of Action	Coordination and Support Actions (CSA)
Indicative EU budget	1 M€
Expected EU contribution per project	The JU estimates that an EU contribution of around EUR 1 million would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	No co-financing by Chips JU Participating States following Article 141(2) SBA One stage Call with submission of Full Proposal (FPP)
Call launch date	08 Jul 2025
Deadline FPP Stage	17 Sep 2025 at 17:00 Brussels Time

4.4.1.1 Context

This support action will help to better connect running and planned semiconductor R&I actions in both regions and to conceive follow-up actions for future joint R&I.

4.4.1.2 Expected Outcomes

- Coordinate ongoing Japanese and EU R&I activities on life cycle assessment (LCA) of semiconductor manufacturing processes and facilitate exchange of researchers to improve coherence.
- Support joint R&I activities between the EU and Japan
- Contribute to preparing potential future joint EU-Japan R&I collaboration topics in the field of semiconductors.
- Explore opportunities to finance talent exchanges between R&D or production sites in both regions.

- Foster increased cooperation with appropriate research institutions in Japan on the development, deployment and commercialisation of digital technologies, for example through specific collaboration in the field of R&I.
- Support joint activities of companies in the semiconductor value chain to improve security of supply for chips.

4.4.1.3 Scope

The scope includes, but is not limited to, the following areas:

- Organize and support networks, conferences, workshops and other actions that:
  - support semiconductor joint EU-Japan R&I activities, in particular to generate R&I priorities for potential future collaboration.
  - Connect EU and Japanese companies in the semiconductor value chain to exchange information and propose measures to improve chip supply chain stability.
- Support exchange of researchers and closer coordination of running R&I activities in both regions which address equal or similar objectivities, for instance on the development of a reference database for Life Cycle Assessment or Green House Gas emission in semiconductor manufacturing processes.
- Increased networking and collaboration of stakeholders from the EU and Japan with a view to addressing current needs, considering future requirements and stimulating long-term cooperation.
- The action should ensure that relevant stakeholders from both the EU and Japan are engaged during the process through regional and international workshops and a set of communication and dissemination actions.

4.4.1.4 Admissibility

Admissibility conditions are described in Annex 1 “HORIZON Europe conditions applicable to Chips JU” of the WP General Annexes.

Regarding page limits:

Chapter	FPP Stage
Excellence	30 pages

Impact	30 pages
Quality and efficiency of the Implementation	60 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

4.4.1.5 Eligibility

Participant eligibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Specific eligibility conditions:

Subject to restrictions for the protection of European communication networks (see Annex 1 of the WP General Annexes for details)

4.4.1.6 Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

4.4.1.7 Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

For the priority order of proposals with the same score, please refer to Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

4.4.1.8 Award criteria.

Award criteria are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

4.4.1.9 Scores

The scores will be given with a resolution of one decimal.

Criteria	Range	Weight (**)	Threshold (*)
Excellence	0-5	1.0	3
Impact	0-5	1.0	3
Quality and efficiency of the implementation	0-5	1.0	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

4.4.1.10 Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to HE.

Type of beneficiary	EU Contribution as % of the Eligible Cost according to HE (*)
For profit organization	100%
SME (for profit SME)	100%
University/Other (not for profit)	100%

(*) beneficiaries may ask for a lower contribution.